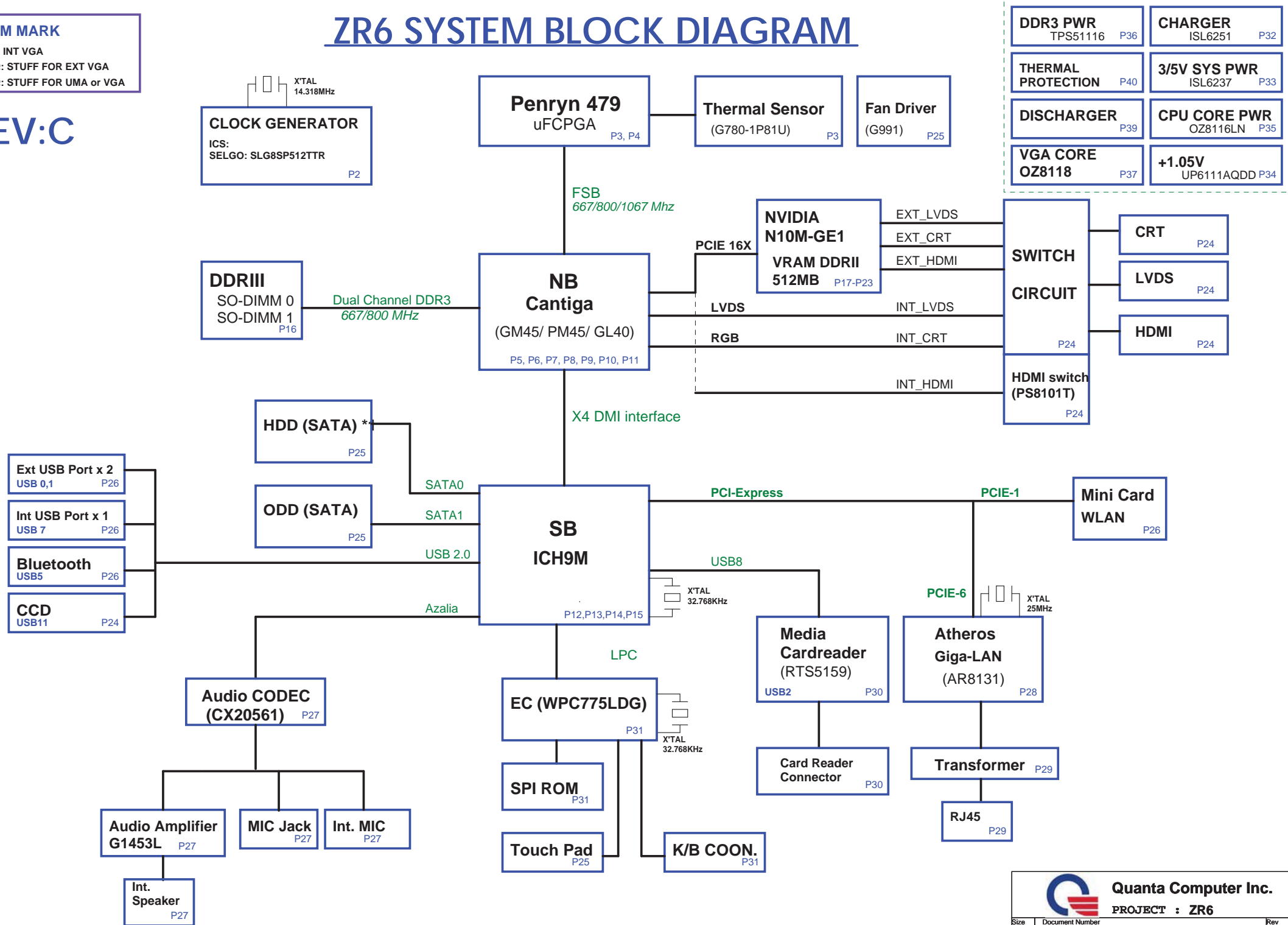


ZR6 SYSTEM BLOCK DIAGRAM

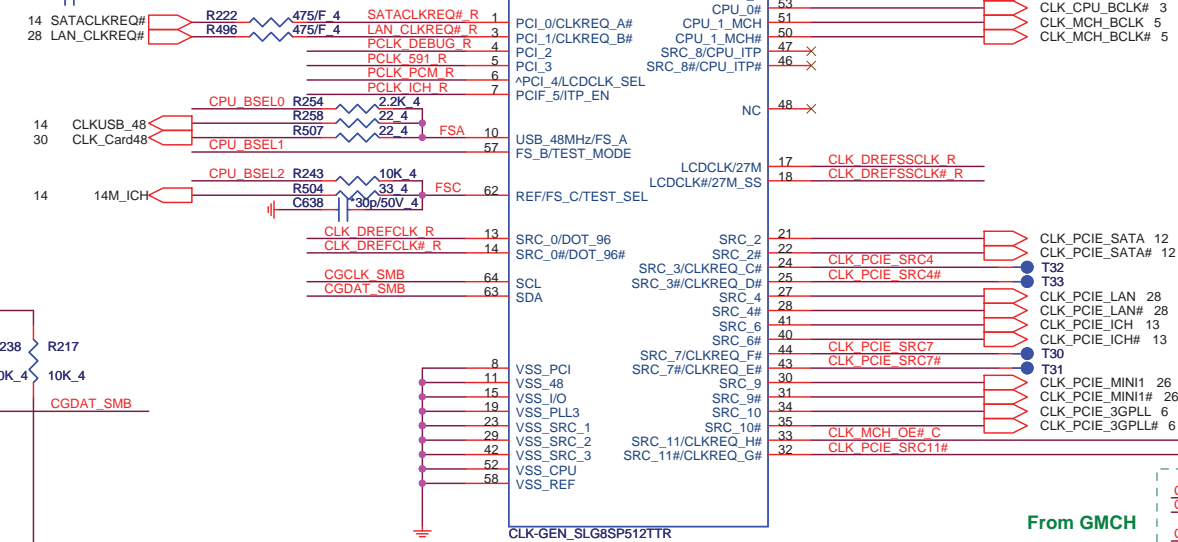
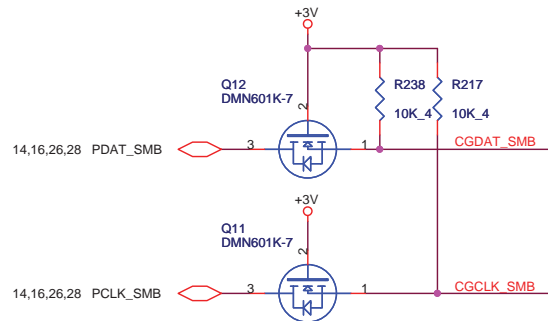
BOM MARK

IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

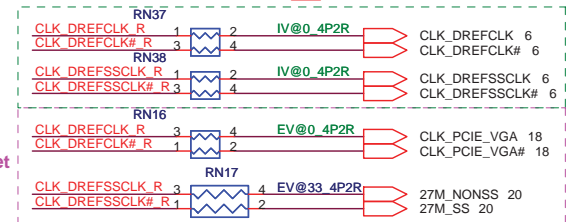
REV:C



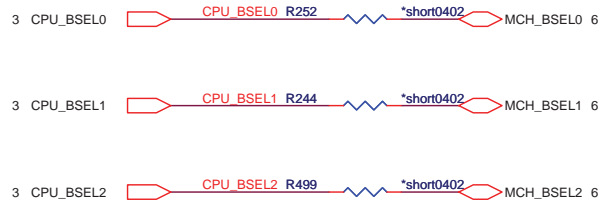
C647	*10p/50V_4 PCLK_DEBUG_R
C371	*10p/50V_4 PCLK_591_R
C641	*10p/50V_4 PCLK_ICH_R
C648	*10p/50V_4 FSA



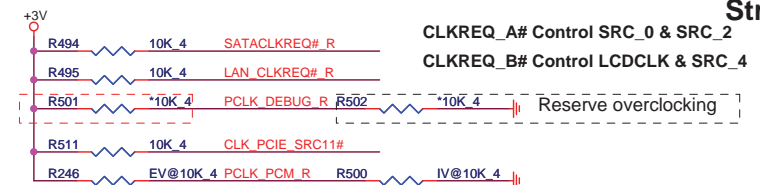
Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.



Pin 10/57/62 : For Pin CPU frequency selection



FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS & SRC_0 for external graphic controller support

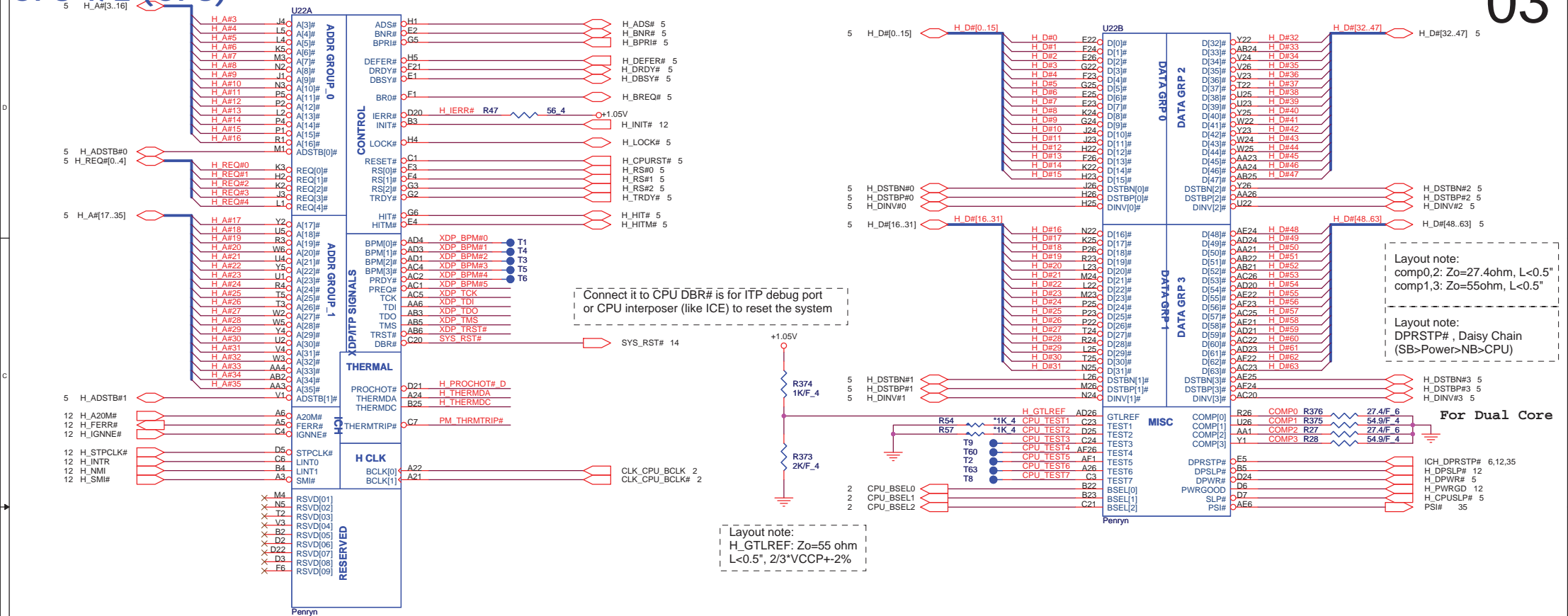
Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

Strap table



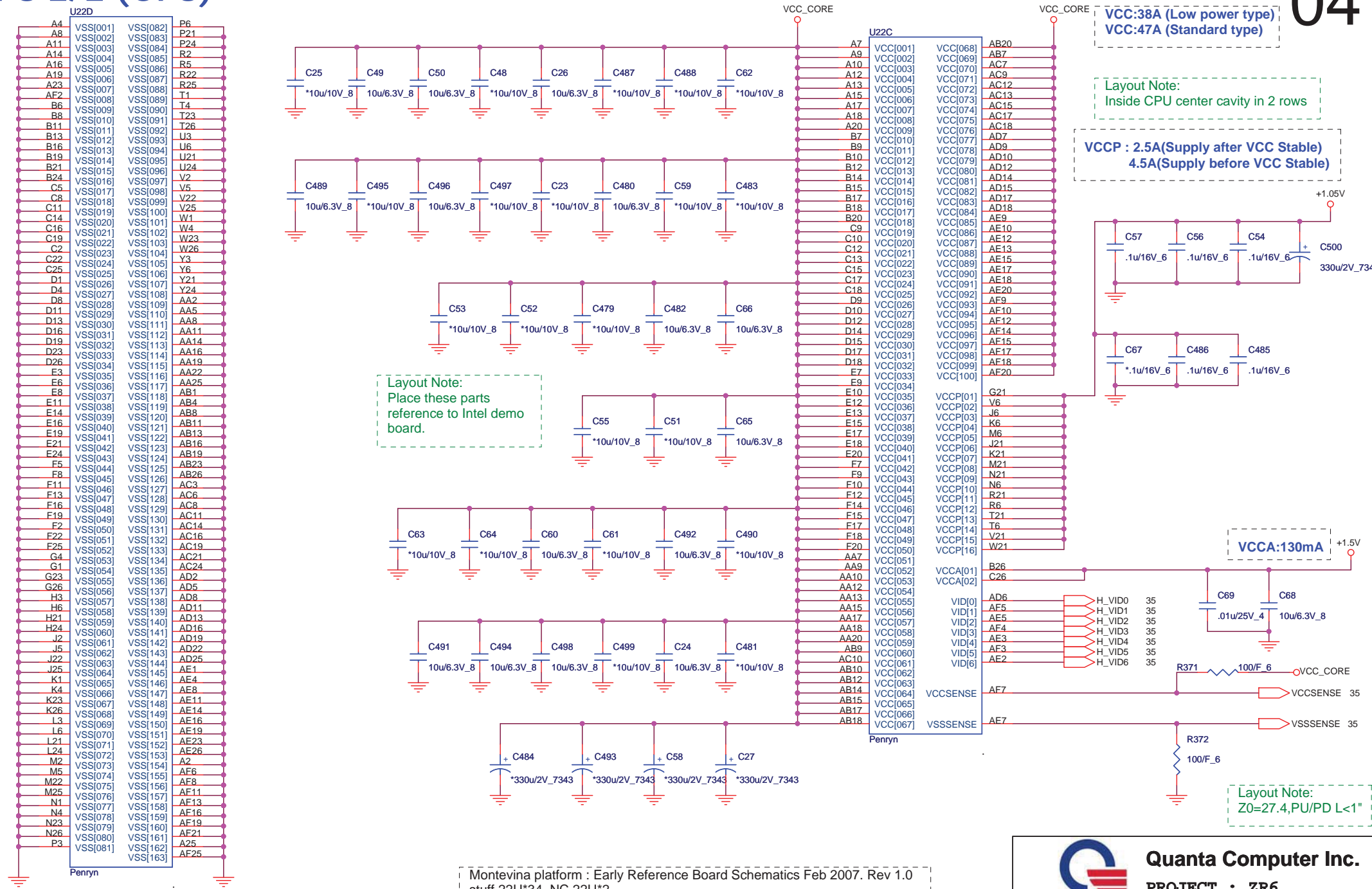
Quanta Computer Inc.
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Size	Document Number	Rev
	CLOCK GENERATOR	1A
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CPU 2/2 (CPU)

04



Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

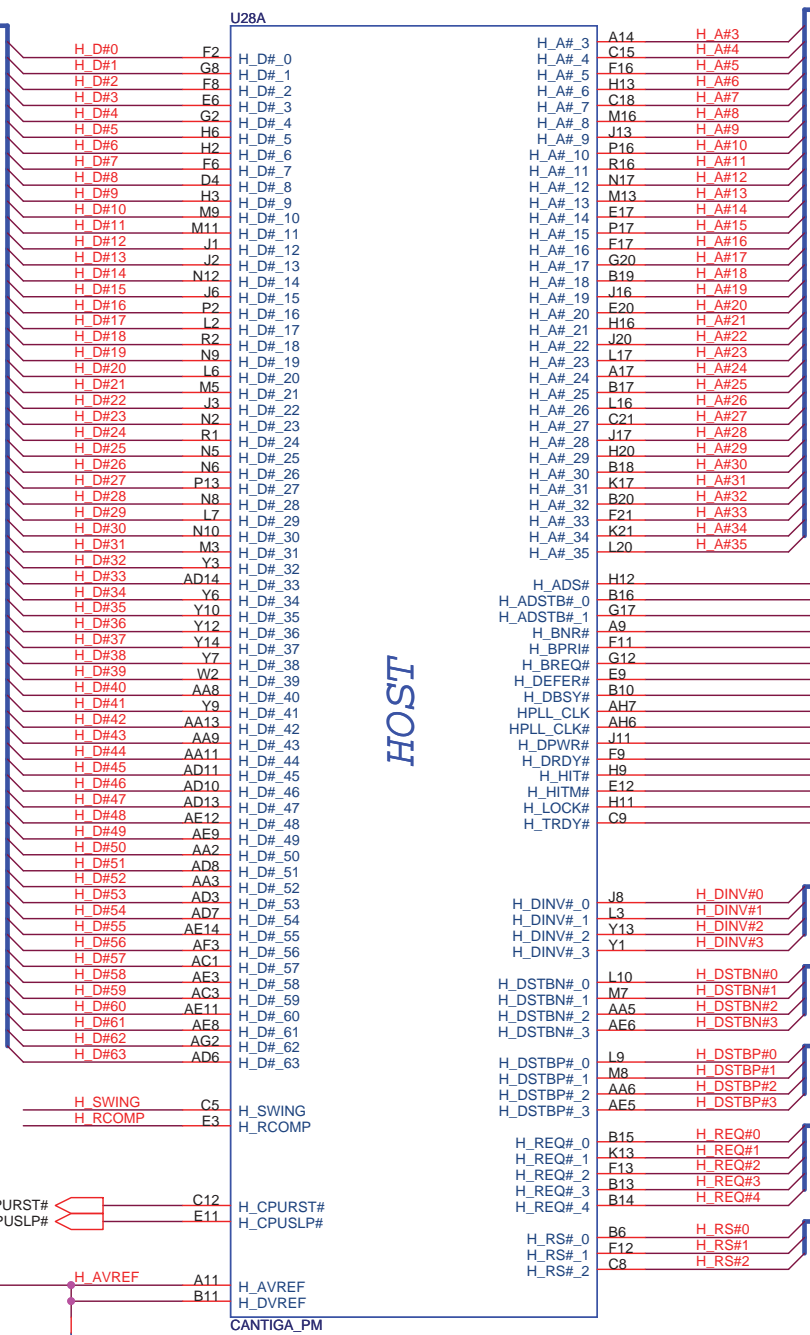
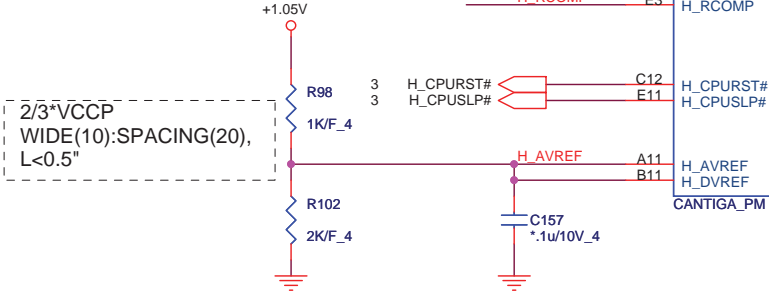
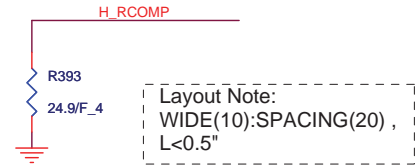
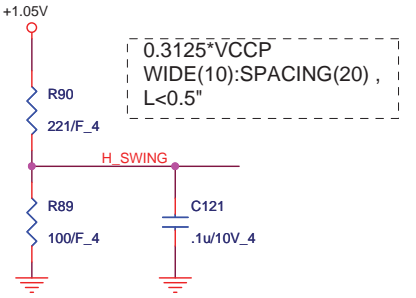


Quanta Computer Inc.
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CPU Power


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GMCH-CANTIGA(CLG)

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



HOST



Quanta Computer Inc.

PROJECT : ZR6

GMCH HOST

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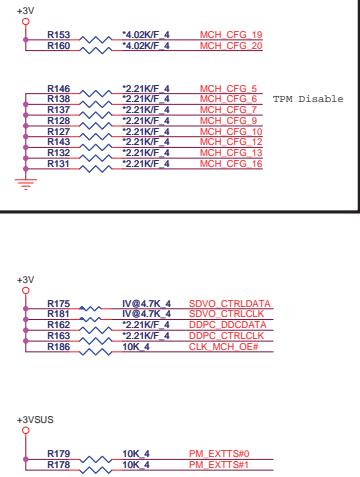
GMCH-CANTIGA(CLG)

IV@
EV@

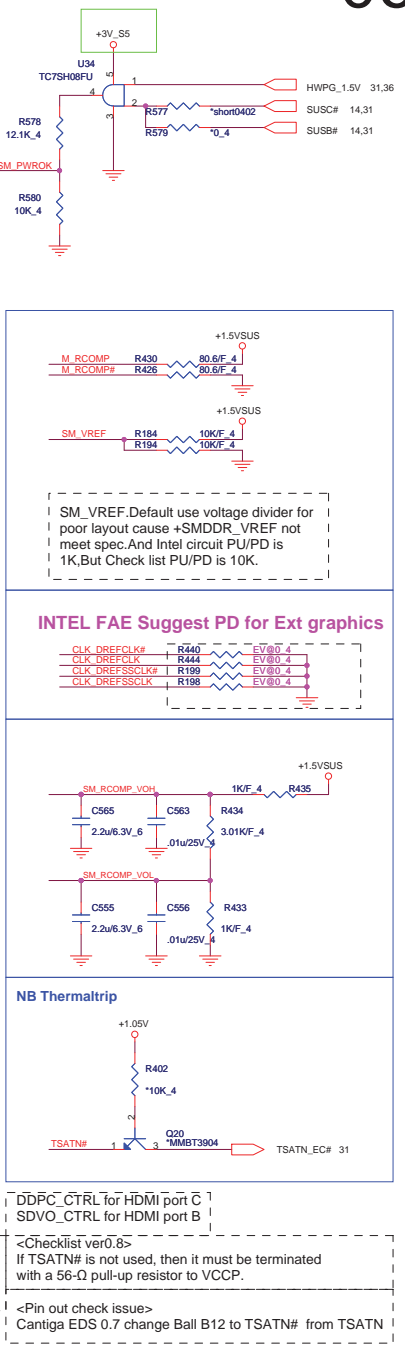
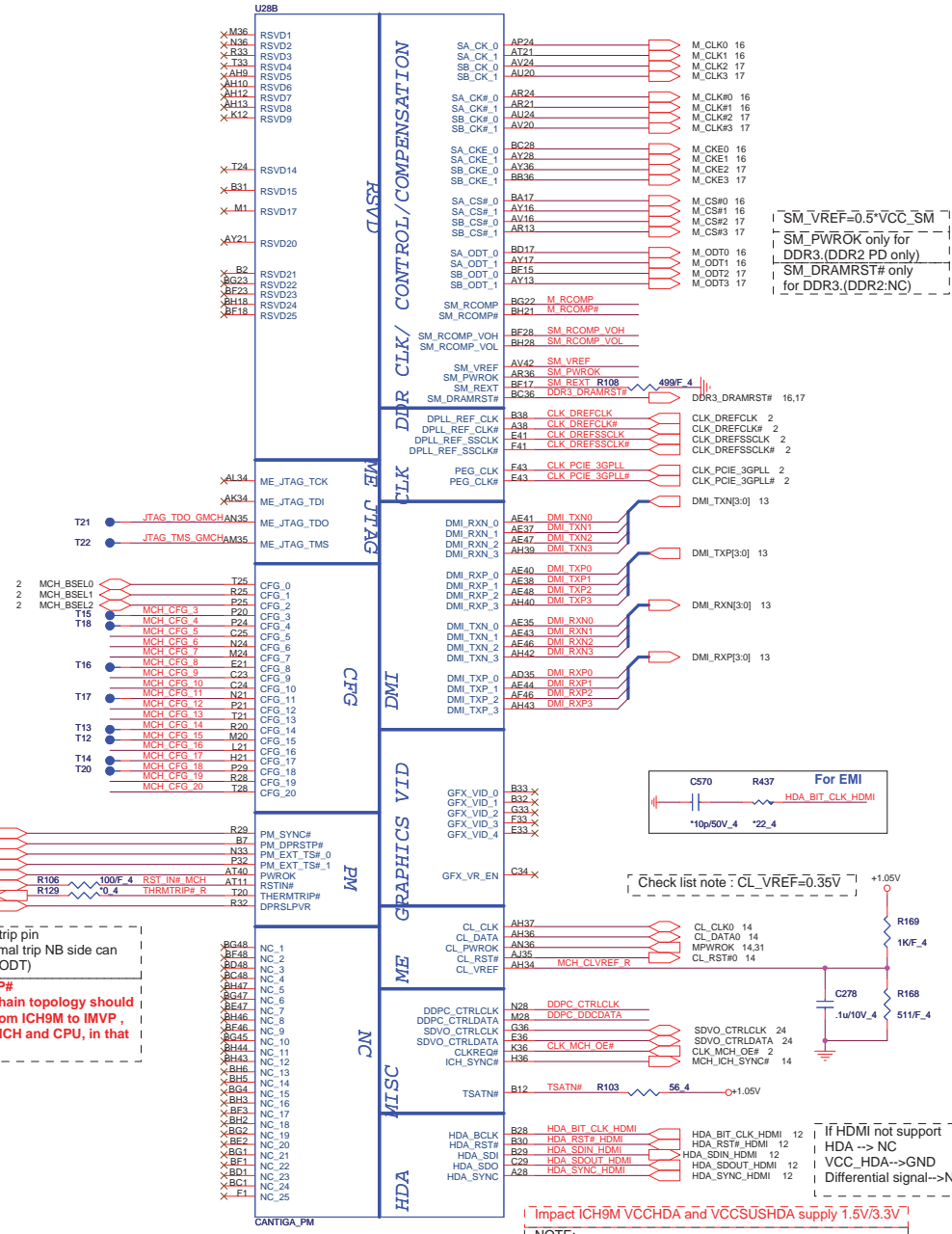
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 106MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin

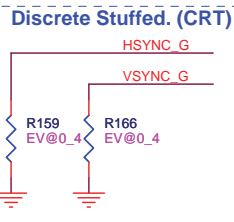
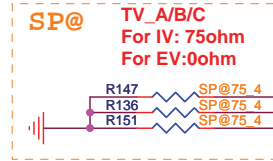


NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)
PM DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.



07

IV@
EV@
SP@



28C	
L_BKLT_CTRL	
L_BKLT_EN	PEG_COMPI
L_CTRL_CLK	PEG_COMPO
L_CTRL_DATA	
L_DDC_CLK	
L_DDC_DATA	
L_VDD_EN	
LVDS_IBG	PEG_RX#_0
LVDS_VBG	PEG_RX#_1
LVDS_VREFH	PEG_RX#_2
LVDS_VREFL	PEG_RX#_3
LVDSA_CLK#	PEG_RX#_4
LVDSA_CLK	PEG_RX#_5
LVDSB_CLK#	PEG_RX#_6
LVDSB_CLK	PEG_RX#_7
LVDSA_DATA#_0	PEG_RX#_8
LVDSA_DATA#_1	PEG_RX#_9
LVDSA_DATA#_2	PEG_RX#_10
LVDSA_DATA#_3	PEG_RX#_11
LVDSA_DATA_0	PEG_RX#_12
LVDSA_DATA_1	PEG_RX#_13
LVDSA_DATA_2	PEG_RX#_14
LVDSA_DATA_3	PEG_RX#_15
LVDSB_DATA#_0	PEG_RX_0
LVDSB_DATA#_1	PEG_RX_1
LVDSB_DATA#_2	PEG_RX_2
LVDSB_DATA#_3	PEG_RX_3
LVDSB_DATA#_0	PEG_RX_4
LVDSB_DATA#_1	PEG_RX_5
LVDSB_DATA#_2	PEG_RX_6
LVDSB_DATA#_3	PEG_RX_7
LVDSB_DATA_0	PEG_RX_8
LVDSB_DATA_1	PEG_RX_9
LVDSB_DATA_2	PEG_RX_10
LVDSB_DATA_3	PEG_RX_11
LVDSB_DATA_0	PEG_RX_12
LVDSB_DATA_1	PEG_RX_13
LVDSB_DATA_2	PEG_RX_14
LVDSB_DATA_3	PEG_RX_15
TVA_DAC	PEG_TX#_0
TVB_DAC	PEG_TX#_1
TVC_DAC	PEG_TX#_2
TV_RTN	PEG_TX#_3
TV_DCONSEL_0	PEG_TX#_4
TV_DCONSEL_1	PEG_TX#_5
	PEG_TX#_6
	PEG_TX#_7
	PEG_TX#_8
	PEG_TX#_9
	PEG_TX#_10
	PEG_TX#_11
	PEG_TX#_12
	PEG_TX#_13
	PEG_TX#_14
	PEG_TX#_15
CRT_BLUE	PEG_TX_0
CRT_GREEN	PEG_TX_1
CRT_RED	PEG_TX_2
CRT_IRTN	PEG_TX_3
CRT_DDC_CLK	PEG_TX_4
CRT_DDC_DATA	PEG_TX_5
CRT_HSYNC	PEG_TX_6
CRT_TV0_IREF	PEG_TX_7
CRT_VSYNC	PEG_TX_8
	PEG_TX_9
	PEG_TX_10
	PEG_TX_11
	PEG_TX_12
	PEG_TX_13
	PEG_TX_14
	PEG_TX_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

PEG_TX	J42	C	PEG_TXP0	C580	.1u/10V 4	PEG_TXP0
PEG_TX_0	L46	C <td>PEG_TXP1 <td>C585</td> <td>.1u/10V 4 <td>PEG_TXP1</td> </td></td>	PEG_TXP1 <td>C585</td> <td>.1u/10V 4 <td>PEG_TXP1</td> </td>	C585	.1u/10V 4 <td>PEG_TXP1</td>	PEG_TXP1
PEG_TX_1	M48	C <td>PEG_TXP2 <td>C590</td> <td>.1u/10V 4 <td>PEG_TXP2</td> </td></td>	PEG_TXP2 <td>C590</td> <td>.1u/10V 4 <td>PEG_TXP2</td> </td>	C590	.1u/10V 4 <td>PEG_TXP2</td>	PEG_TXP2
PEG_TX_2	M39	C <td>PEG_TXP3 <td>C597</td> <td>.1u/10V 4 <td>PEG_TXP3</td> </td></td>	PEG_TXP3 <td>C597</td> <td>.1u/10V 4 <td>PEG_TXP3</td> </td>	C597	.1u/10V 4 <td>PEG_TXP3</td>	PEG_TXP3
PEG_TX_3	M43	C <td>PEG_TXP4 <td>C611</td> <td>EV@.1U/10V 4 <td>PEG_TXP4</td> </td></td>	PEG_TXP4 <td>C611</td> <td>EV@.1U/10V 4 <td>PEG_TXP4</td> </td>	C611	EV@.1U/10V 4 <td>PEG_TXP4</td>	PEG_TXP4
PEG_TX_4	R47	C <td>PEG_TXP5 <td>C586</td> <td>EV.1U/10V 4 <td>PEG_TXP5</td> </td></td>	PEG_TXP5 <td>C586</td> <td>EV.1U/10V 4 <td>PEG_TXP5</td> </td>	C586	EV.1U/10V 4 <td>PEG_TXP5</td>	PEG_TXP5
PEG_TX_5	N37	C <td>PEG_TXP6 <td>C601</td> <td>EV@.1U/10V 4 <td>PEG_TXP6</td> </td></td>	PEG_TXP6 <td>C601</td> <td>EV@.1U/10V 4 <td>PEG_TXP6</td> </td>	C601	EV@.1U/10V 4 <td>PEG_TXP6</td>	PEG_TXP6
PEG_TX_6	T39	C <td>PEG_TXP7 <td>C599</td> <td>EV.1U/10V 4 <td>PEG_TXP7</td> </td></td>	PEG_TXP7 <td>C599</td> <td>EV.1U/10V 4 <td>PEG_TXP7</td> </td>	C599	EV.1U/10V 4 <td>PEG_TXP7</td>	PEG_TXP7
PEG_TX_7	U36	C <td>PEG_TXP8 <td>C605</td> <td>EV@.1U/10V 4 <td>PEG_TXP8</td> </td></td>	PEG_TXP8 <td>C605</td> <td>EV@.1U/10V 4 <td>PEG_TXP8</td> </td>	C605	EV@.1U/10V 4 <td>PEG_TXP8</td>	PEG_TXP8
PEG_TX_8	U39	C <td>PEG_TXP9 <td>C602</td> <td>EV.1U/10V 4 <td>PEG_TXP9</td> </td></td>	PEG_TXP9 <td>C602</td> <td>EV.1U/10V 4 <td>PEG_TXP9</td> </td>	C602	EV.1U/10V 4 <td>PEG_TXP9</td>	PEG_TXP9
PEG_TX_9	Y39	C <td>PEG_TXP10 <td>C609</td> <td>EV@.1U/10V 4 <td>PEG_TXP10</td> </td></td>	PEG_TXP10 <td>C609</td> <td>EV@.1U/10V 4 <td>PEG_TXP10</td> </td>	C609	EV@.1U/10V 4 <td>PEG_TXP10</td>	PEG_TXP10
PEG_TX_10	Y46	C <td>PEG_TXP11 <td>C595</td> <td>EV.1U/10V 4 <td>PEG_TXP11</td> </td></td>	PEG_TXP11 <td>C595</td> <td>EV.1U/10V 4 <td>PEG_TXP11</td> </td>	C595	EV.1U/10V 4 <td>PEG_TXP11</td>	PEG_TXP11
PEG_TX_11	AA36	C <td>PEG_TXP12 <td>C617</td> <td>EV@.1U/10V 4 <td>PEG_TXP12</td> </td></td>	PEG_TXP12 <td>C617</td> <td>EV@.1U/10V 4 <td>PEG_TXP12</td> </td>	C617	EV@.1U/10V 4 <td>PEG_TXP12</td>	PEG_TXP12
PEG_TX_12	AA39	C <td>PEG_TXP13 <td>C620</td> <td>EV.1U/10V 4 <td>PEG_TXP13</td> </td></td>	PEG_TXP13 <td>C620</td> <td>EV.1U/10V 4 <td>PEG_TXP13</td> </td>	C620	EV.1U/10V 4 <td>PEG_TXP13</td>	PEG_TXP13
PEG_TX_13	AD42	C <td>PEG_TXP14 <td>C615</td> <td>EV@.1U/10V 4 <td>PEG_TXP14</td> </td></td>	PEG_TXP14 <td>C615</td> <td>EV@.1U/10V 4 <td>PEG_TXP14</td> </td>	C615	EV@.1U/10V 4 <td>PEG_TXP14</td>	PEG_TXP14
PEG_TX_14	AD46	C <td>PEG_TXP15 <td>C592</td> <td>EV@.1U/10V 4 <td>PEG_TXP15</td> </td></td>	PEG_TXP15 <td>C592</td> <td>EV@.1U/10V 4 <td>PEG_TXP15</td> </td>	C592	EV@.1U/10V 4 <td>PEG_TXP15</td>	PEG_TXP15
PEG_TX_15						

SP@

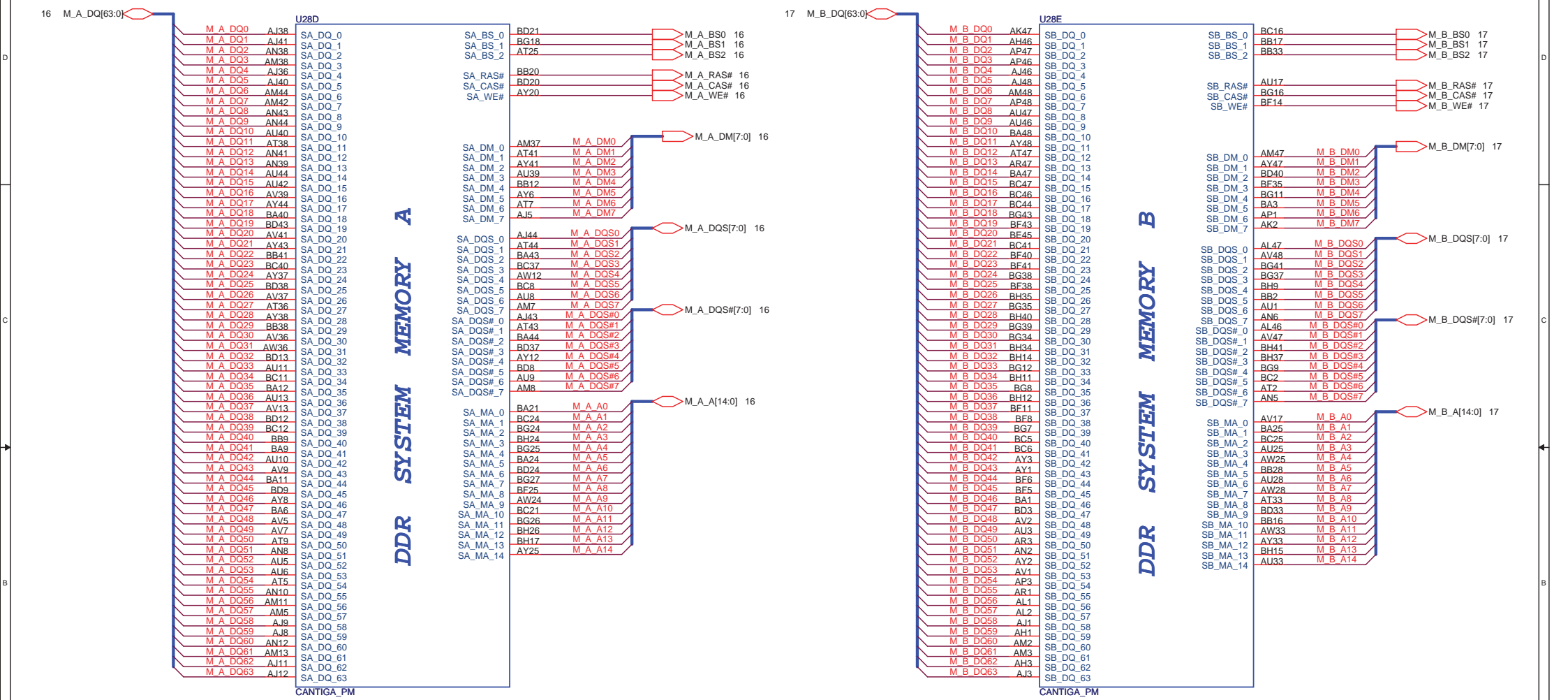
18,24

CRT_R/G/B
For IV: 150ohm
For EV:0ohm


R155 SP@150/F 4 INT CRT BLU

R154 SP@150/F 4 INT CRT GRN

R150 SP@150/F 4 INT CRT RED



09

 <div> Quanta Computer Inc. PROJECT : ZR6 </div>		
Size	Document Number	Rev
	GMCH VCC,NCTF	1/
Date: Monday, April 13, 2009	Sheet 9 of 42	

IV@
EV@
SP@

Power consumption reference to Intel
Cantiga chipset EDS Volume1, Section 10

1210 10uH, 10%
0.45A DCR_max = 0.39

IV&EV Dis/Enable setting

SP@:INT use 0.1U
EXT use 0 ohm

1.05V
64.8mA for DPLL A/B

1210 10uH, 10%
0.45A DCR_max = 0.39

ESR=15 m

1210 0.1uH, 20%, 1A,
DCR_max=0.078Q

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

VCCD_TV_DAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
48.363mA for CRT
5mA for TV

FB 220 @100 MHz, 25%, 2A

MODIFY

IV&EV Dis/Enable setting

1.8V
60.31mA

SP@:INT use 1 U
EXT use 0 ohm

5

4

3

2

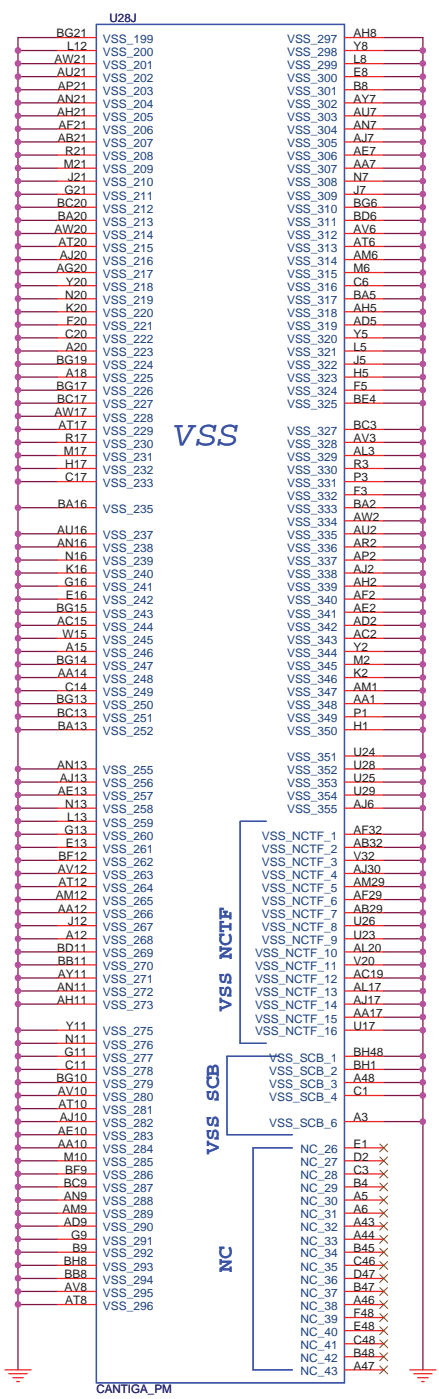
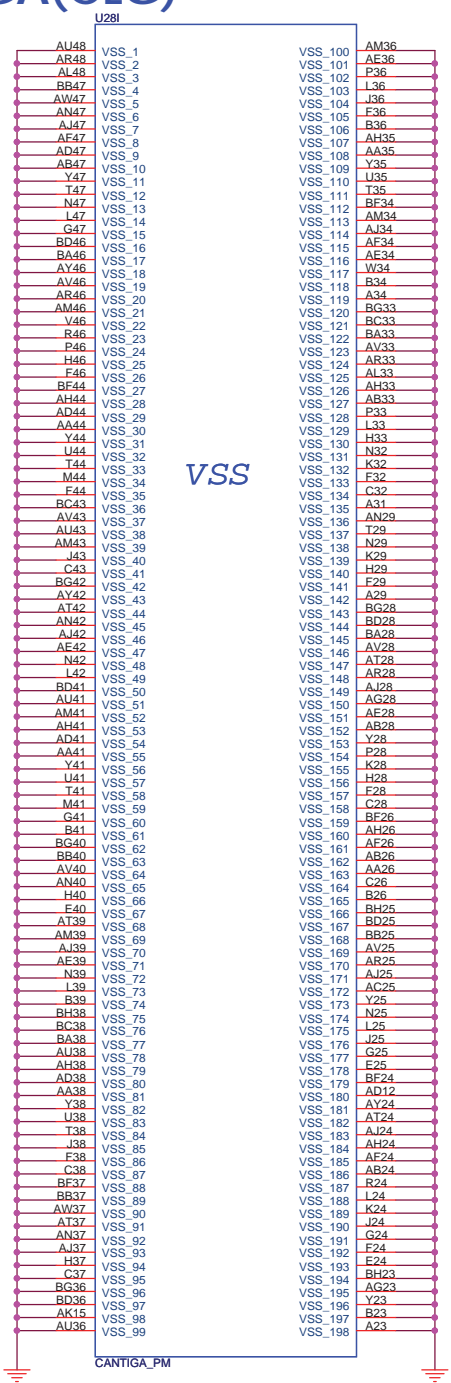
1

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCB_LVDS	GND
VCCD_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

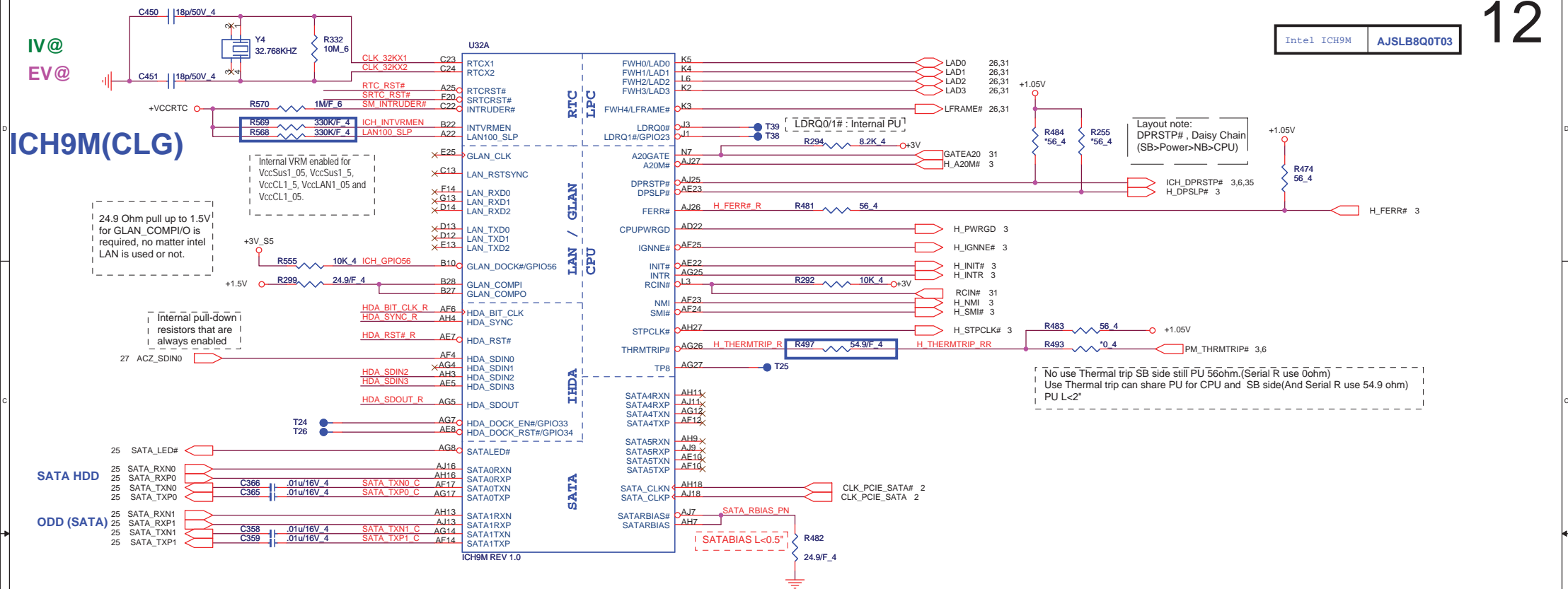
Power Net Name	Cantiga(V)
VCC_AXG_#	1.05V
VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

GMCH-CANTIGA(CLG)

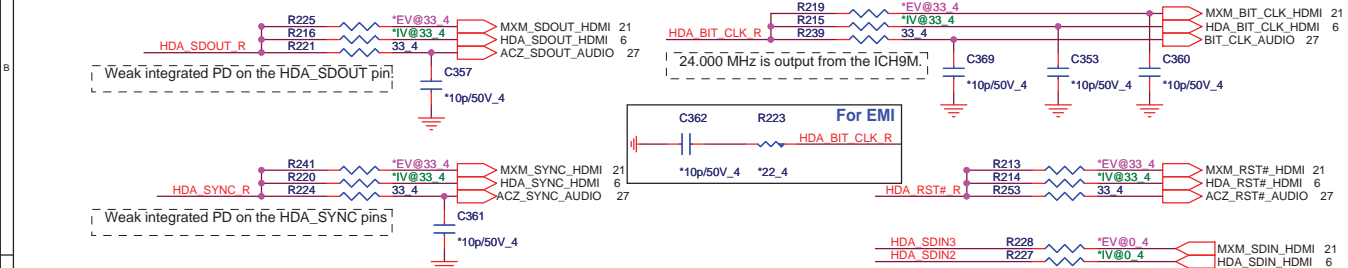


IV@
EV@

ICH9M(CLG)



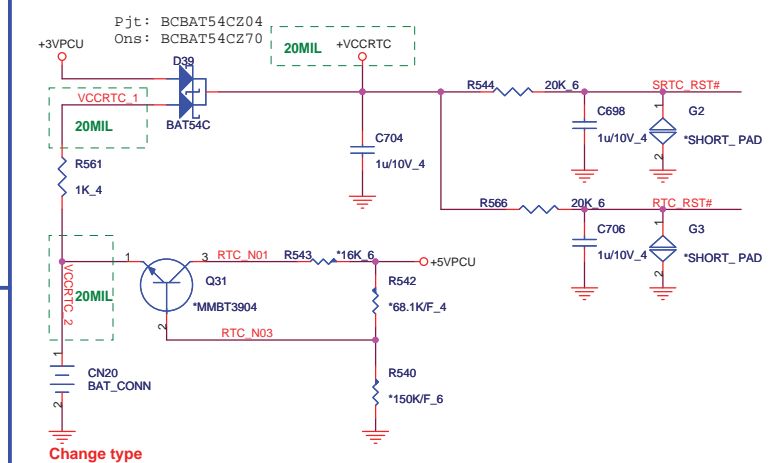
HD Audio

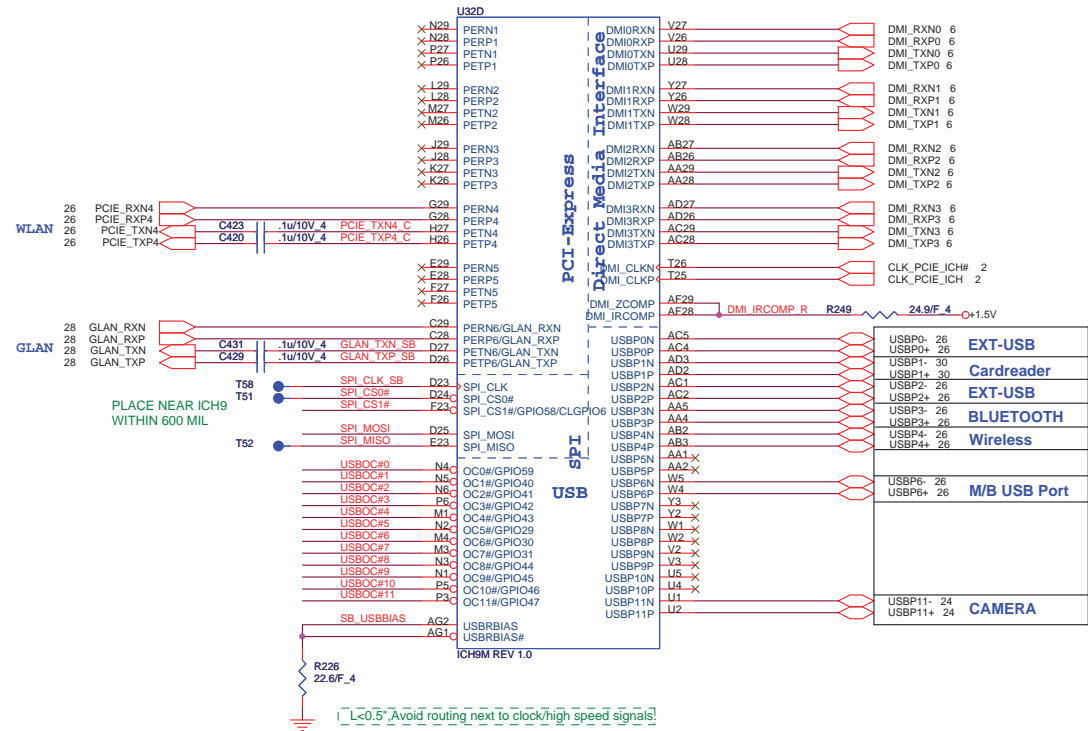


South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration		PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect		This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUR	Description
			0	0	RSVD
			0	1	Enter XOR Chain
HDA_SDOUR	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	1	0	Normal operation(Default)
			1	1	Set PCIe port config bit 1

RTC



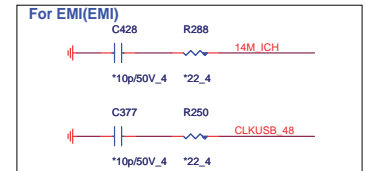


Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

ICH9M(CLG)

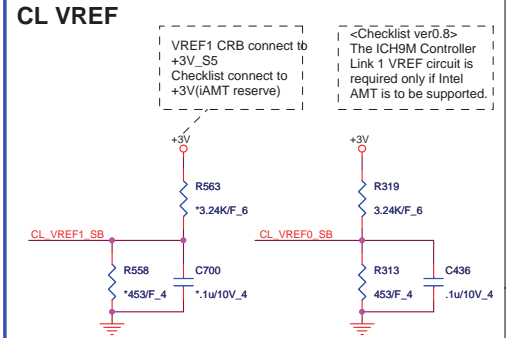
1 D3A:(1/31) ASF issue:when iAMT is not implemented,
1 ICH8M SMBus and SMLink should be connected together to support slave mode
1 Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground

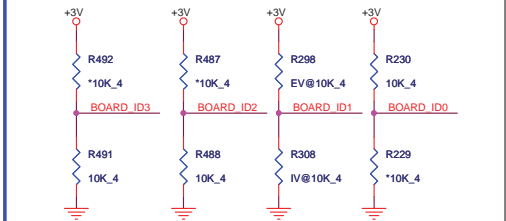


If integrated LAN is not used LAN_RST# tie it to GND. NC serial R from RSMRST#.
 If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs
on the NB and SB on a platform with no IAMT



M/B ID	ID0=0 -->ZK6 , ID0=1 -->ZR6
	ID1=0 -->UMA , ID1=1 -->Discrete

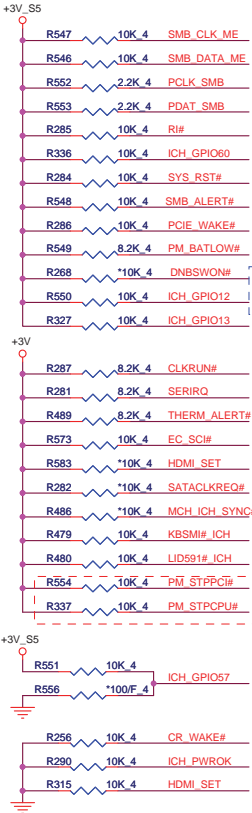


Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

**Quanta Computer Inc.**

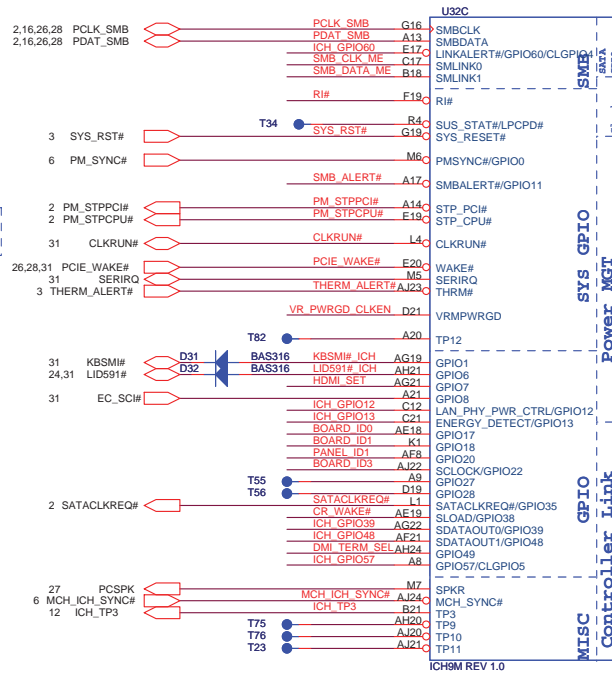
PROJECT : ZR6

Size	Document Number	Rev
	ICH9M GPIO	1A
Date:	Monday, April 13, 2009	Sheet 14 of 42



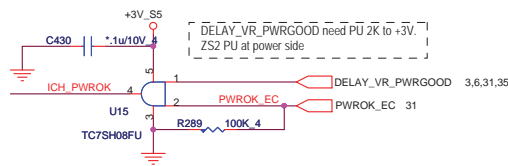
TPM Physical Presence for iTPM.

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

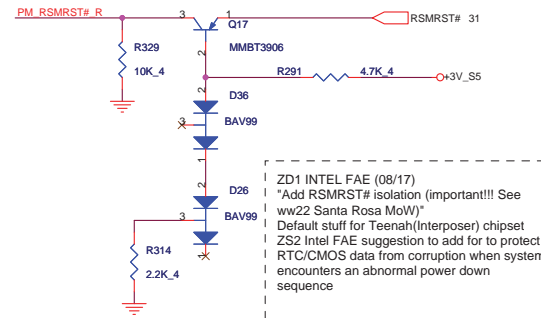


ZS2 Default not
 support IAMT. So this
 interface follow
 CRB/Checklist PU
 only

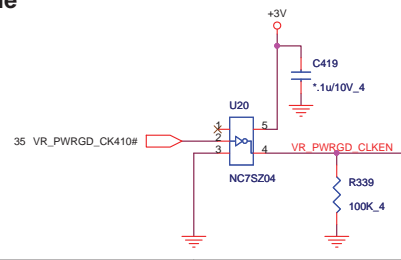
ICH PWROK





Resume RST



CLK Enable



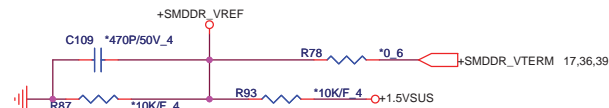
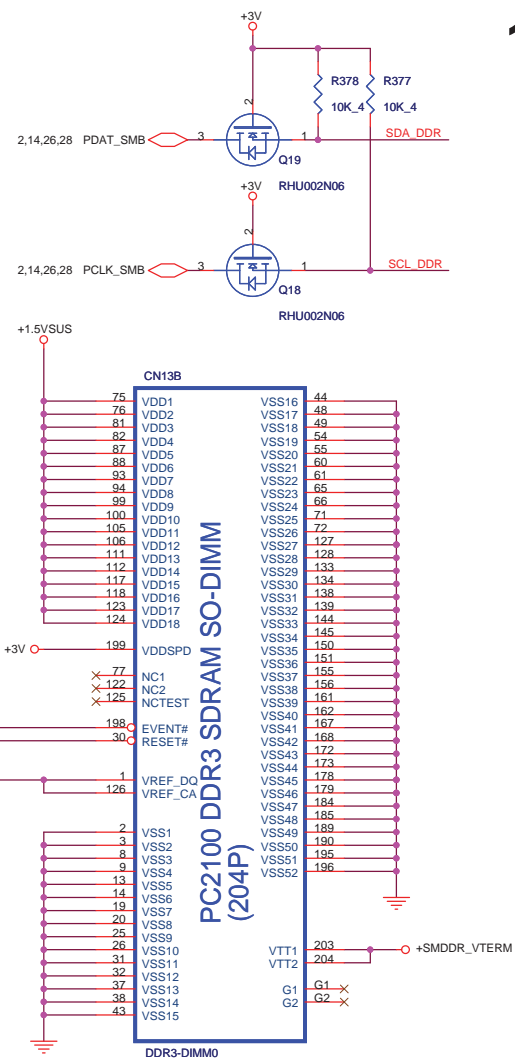
South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	

PER INTEL SUGGESTION:
CHANGE TO 100OHM & 1UF



16

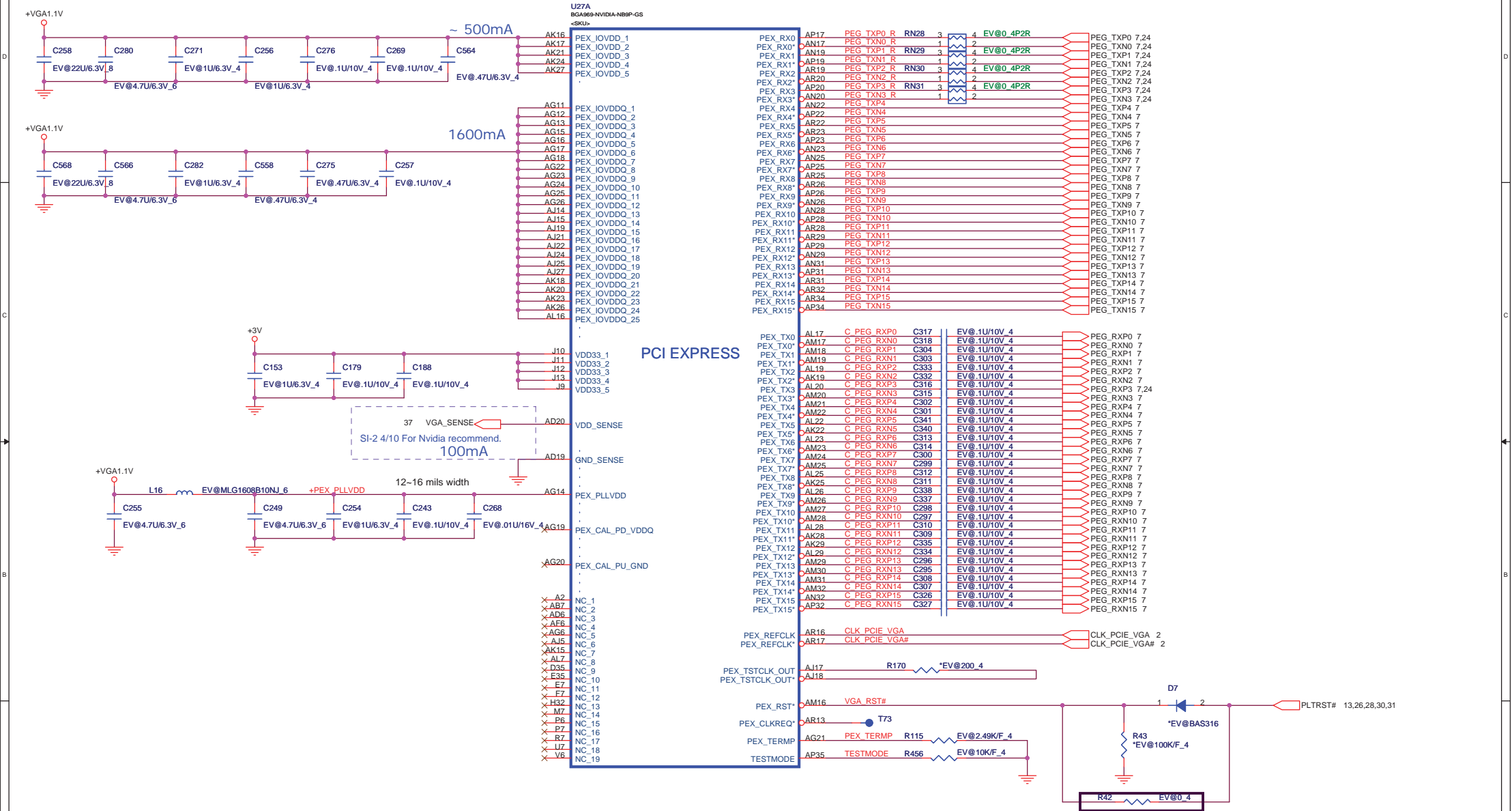




Rev	1A
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12

12

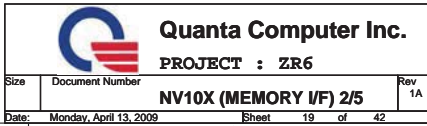


Quanta Computer Inc.

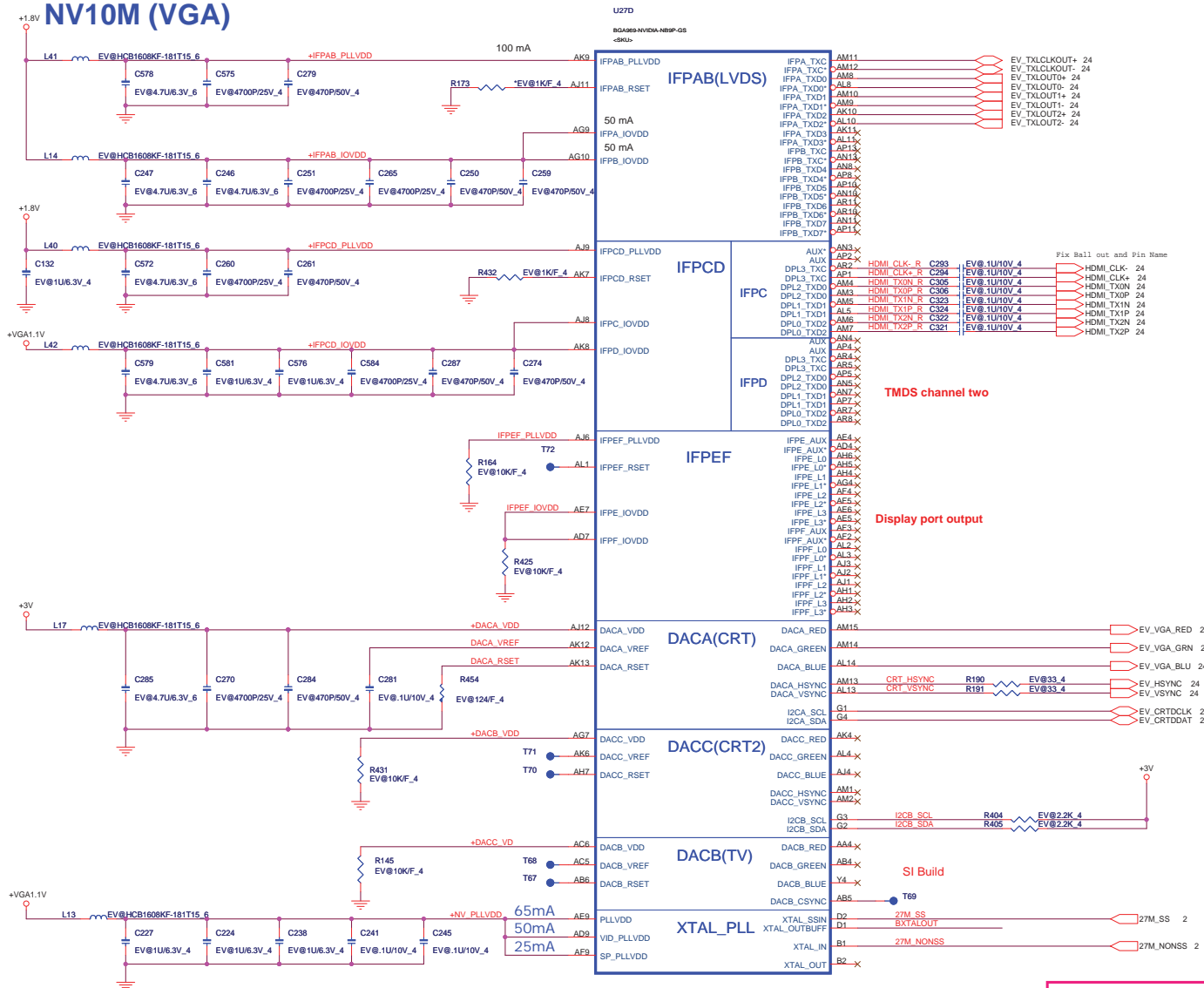
PROJECT : ZR6

Rev 1A

Size	Document Number	Rev
Monday, April 13, 2009	Sheet 18 of 42	1A



NV10M (VGA)

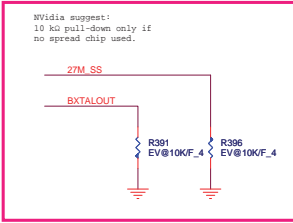


TMD5 channel two

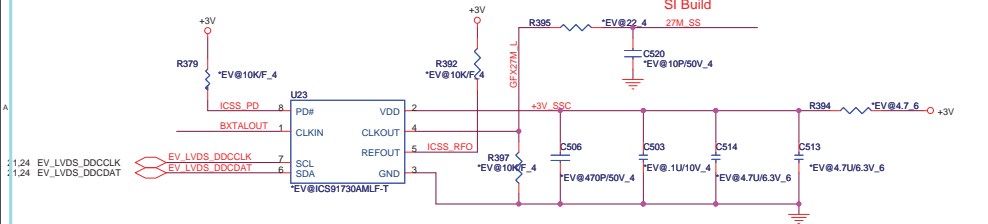
Display port output

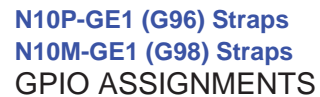


SI Build



SPREAD SPECTRUM





GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



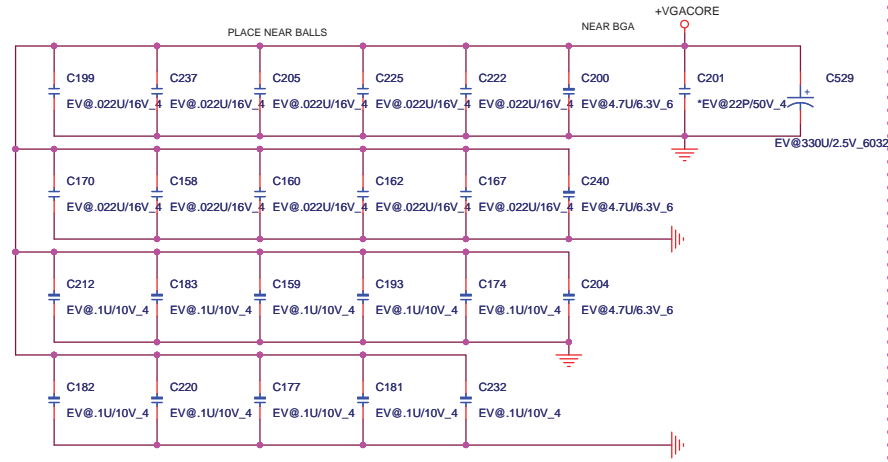
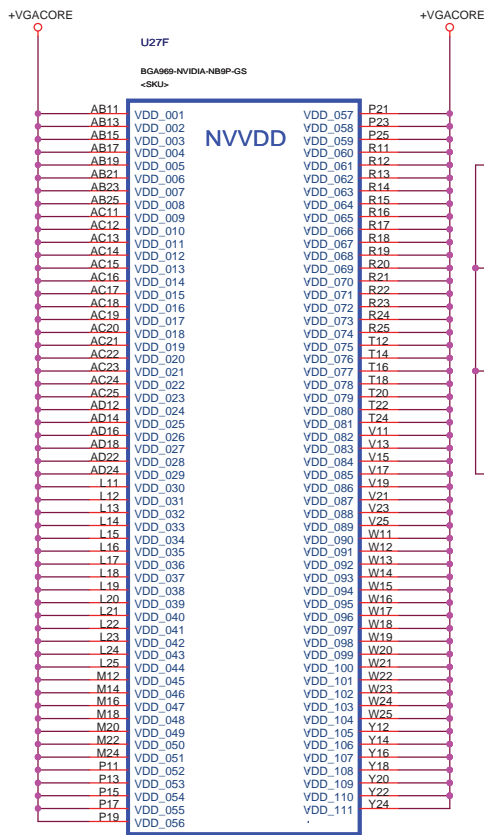
Logical Strap Bit Mapping

R414	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

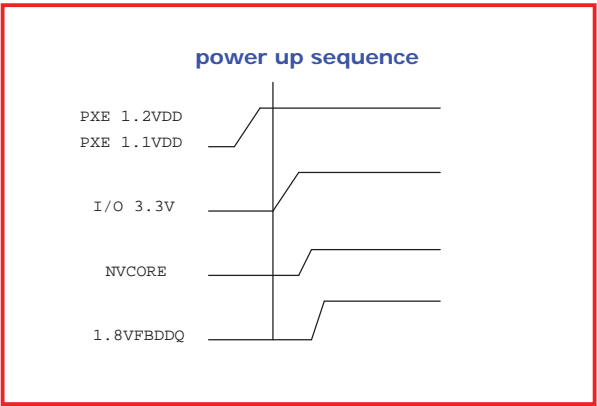
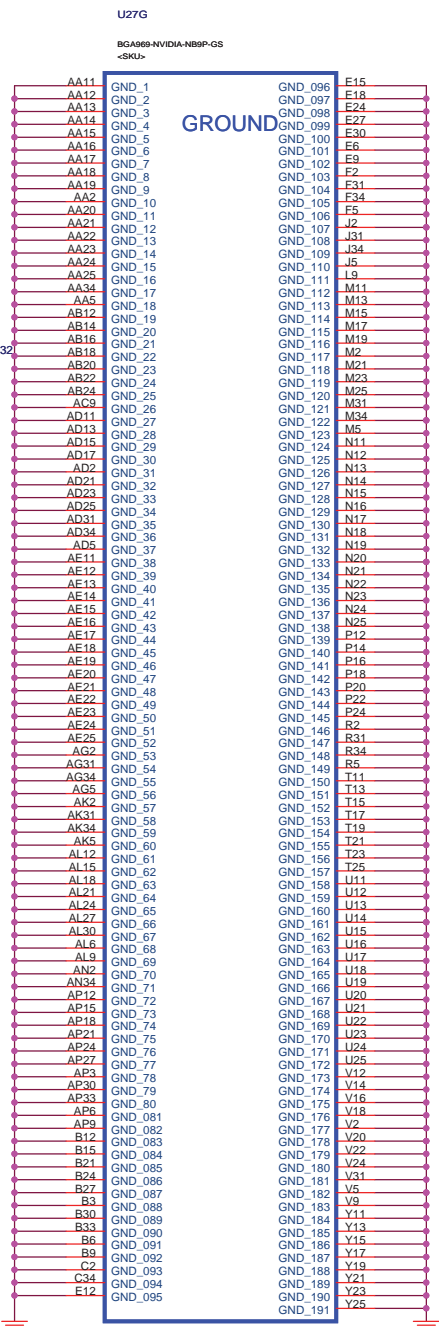
I2C ADDRESS: 0x98H



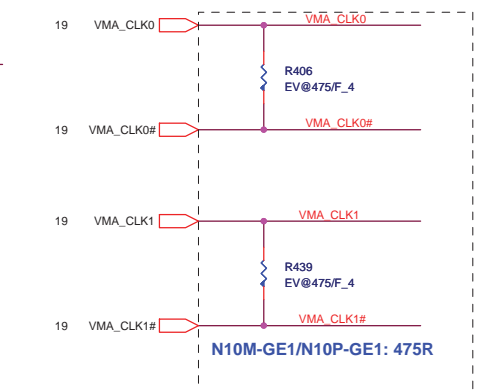
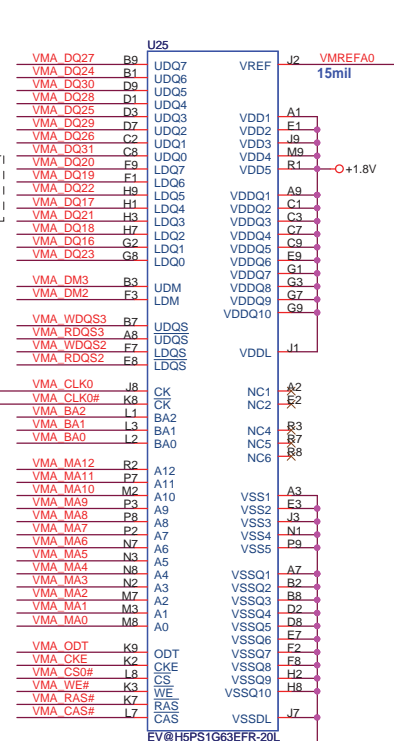
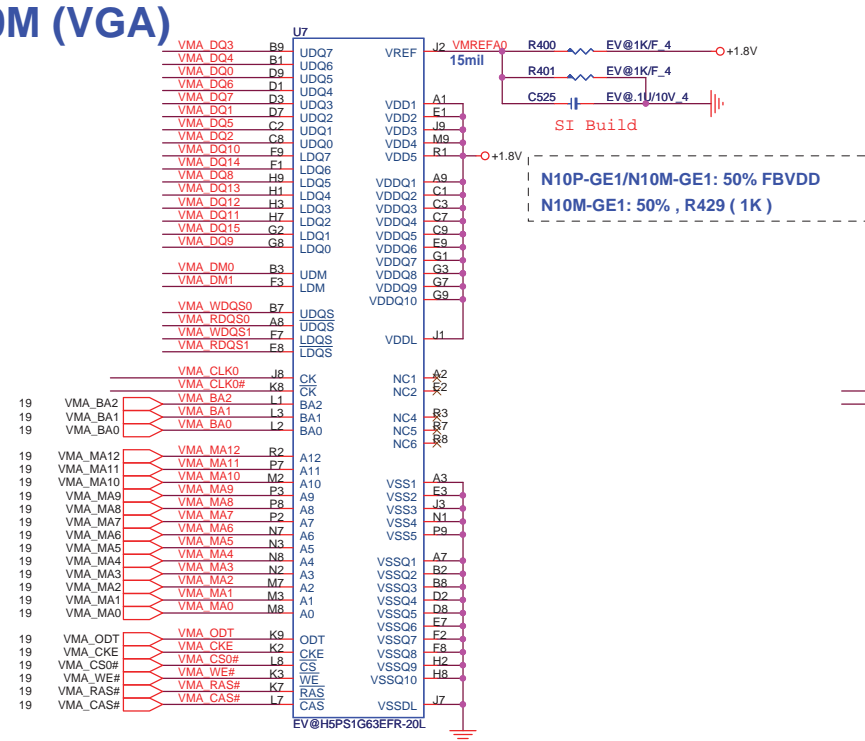
NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10

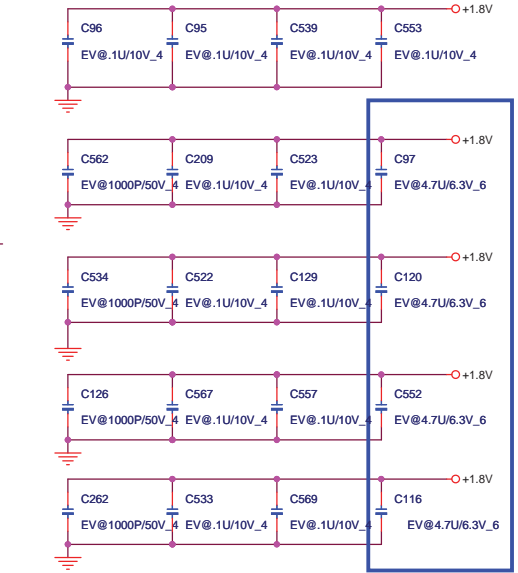


NV10M (VGA)

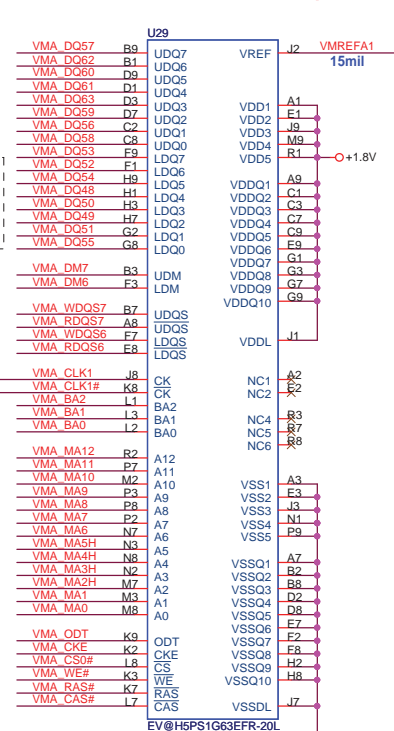
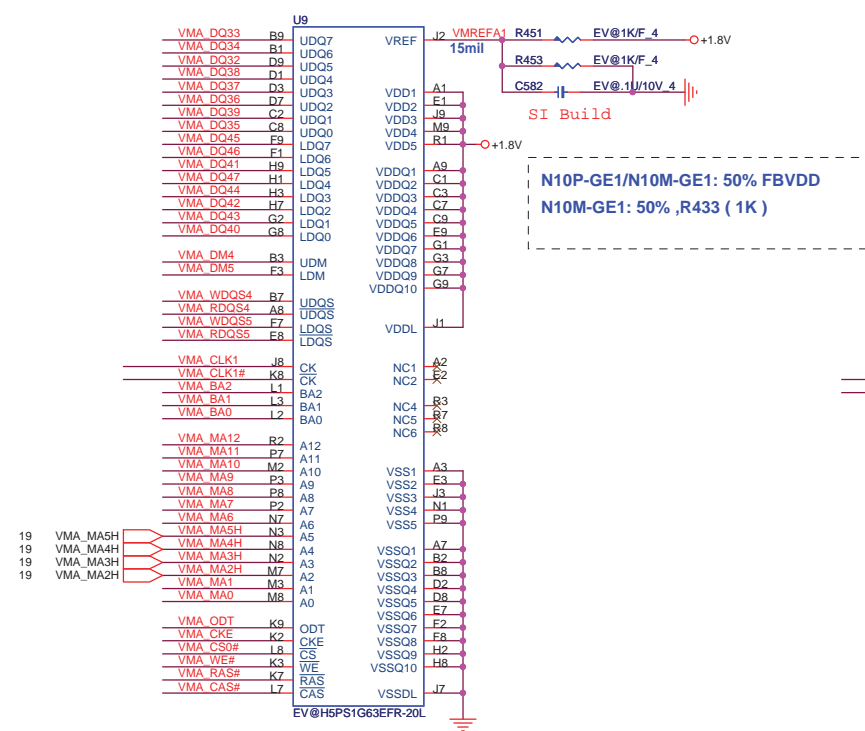


CS14752FB11 RES CHIP 475 1/16W +1%(0402)

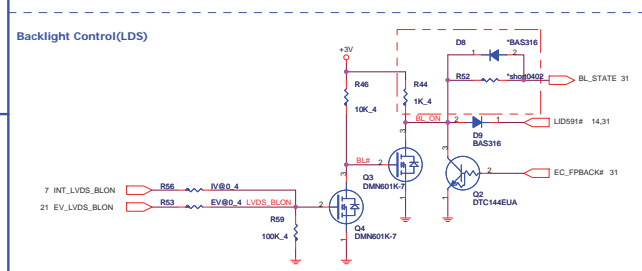
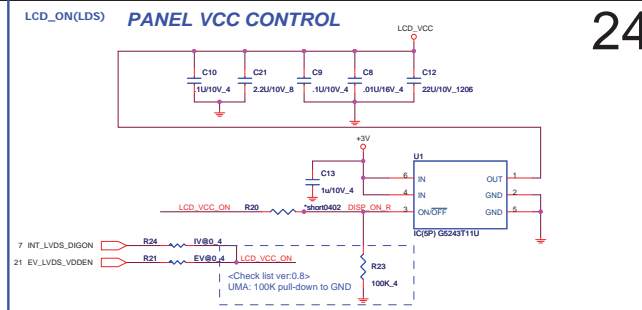
(By pass capacitor)



For DB:
N10P/N10M : AKD5LG-T510(Samsung,64M*16)
AKD5LG-TW02(Hynix,64M*16)



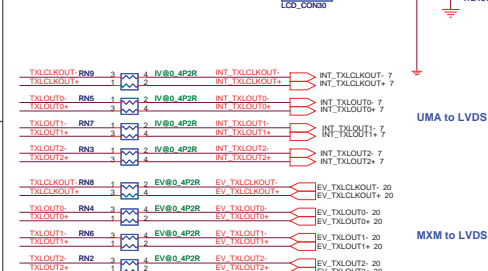
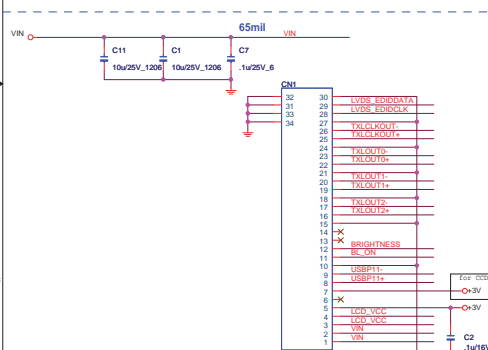
24



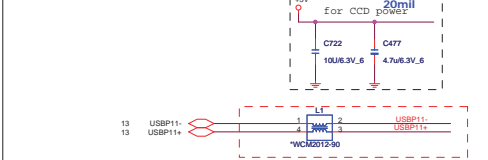
Lid Switch (HSR)



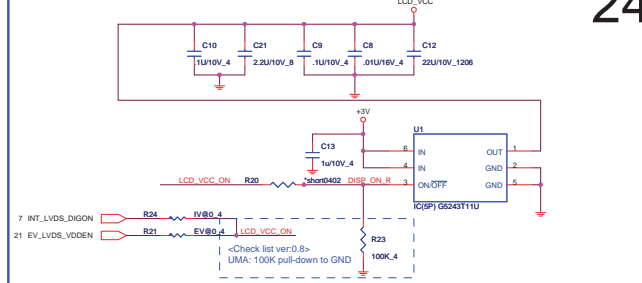
HDMI (HDM)



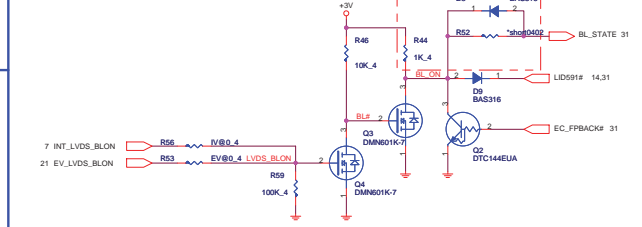
Modify



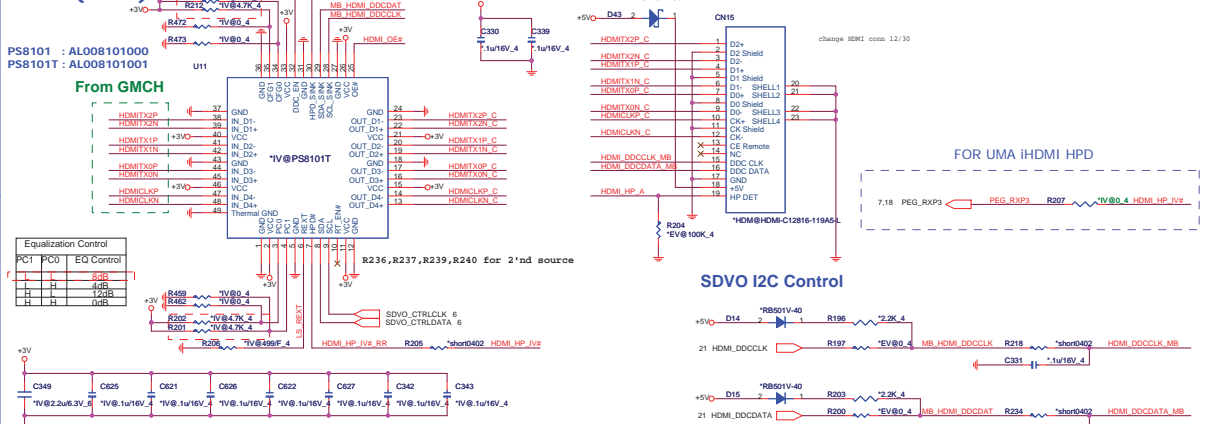
PANEL VCC CONTROL



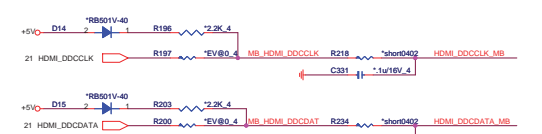
Backlight Control(LDS



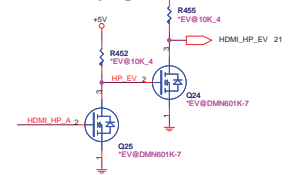
HDMI (HDM)



SDVO I2C Control



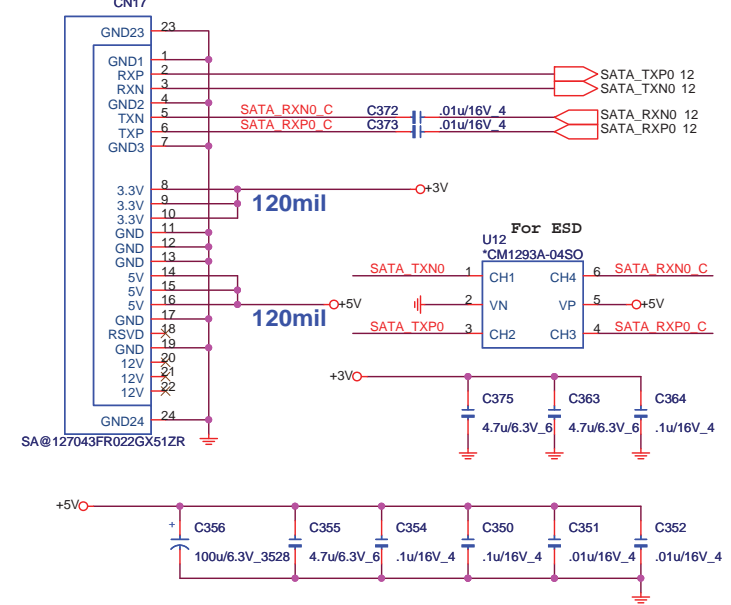
EV@Hot-plug



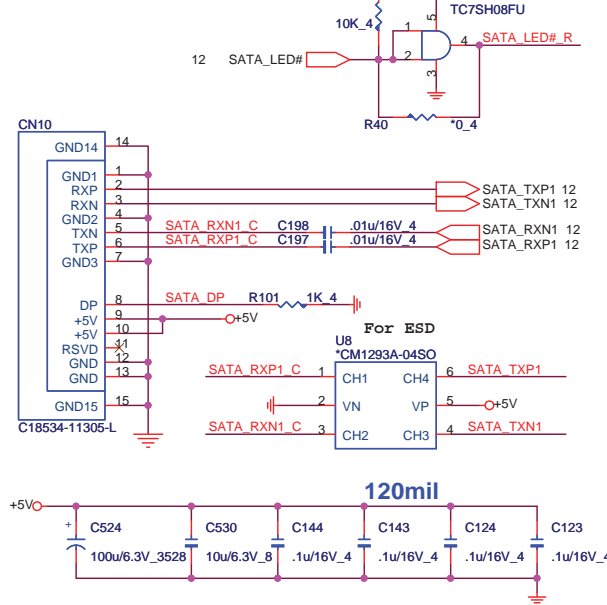
FOR NV HDMI



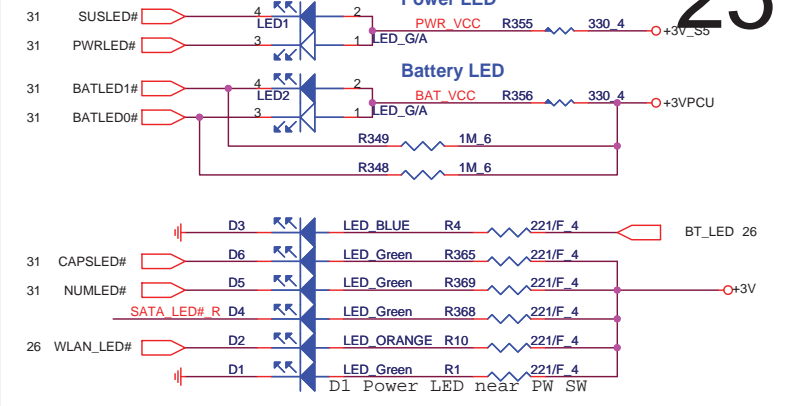
SATA HDD(HDD)



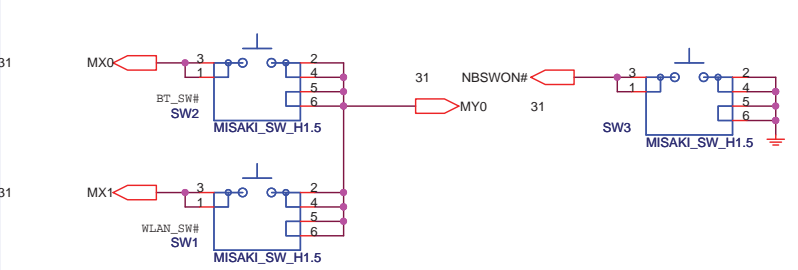
SATA ODD(ODD)



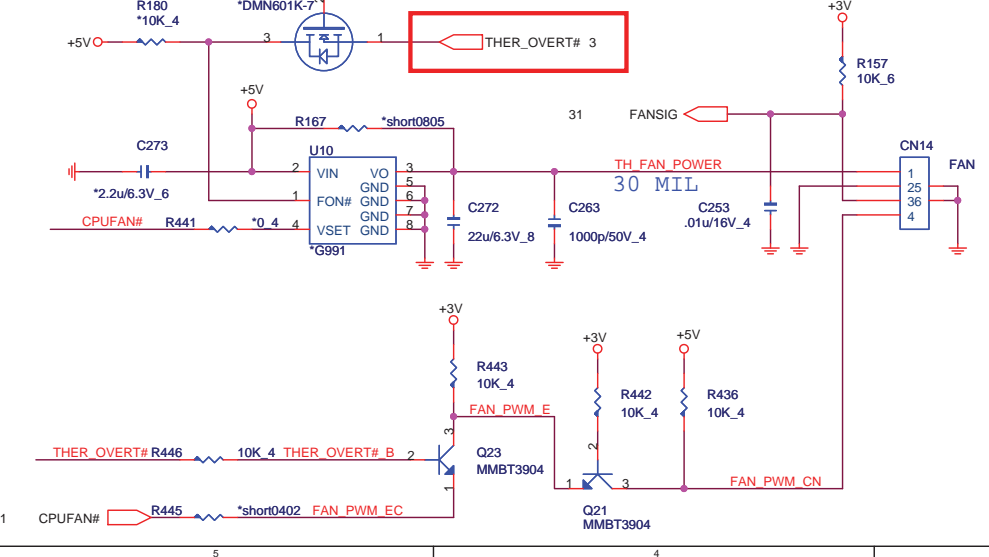
LED(UIF) Power / Suspend: Green / Amber



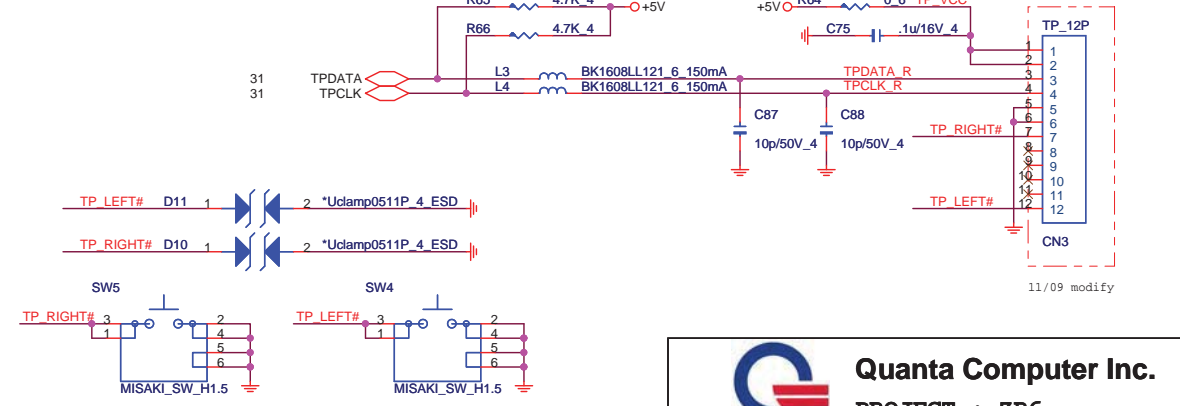
Power Button (UIF)



FAN(THM)

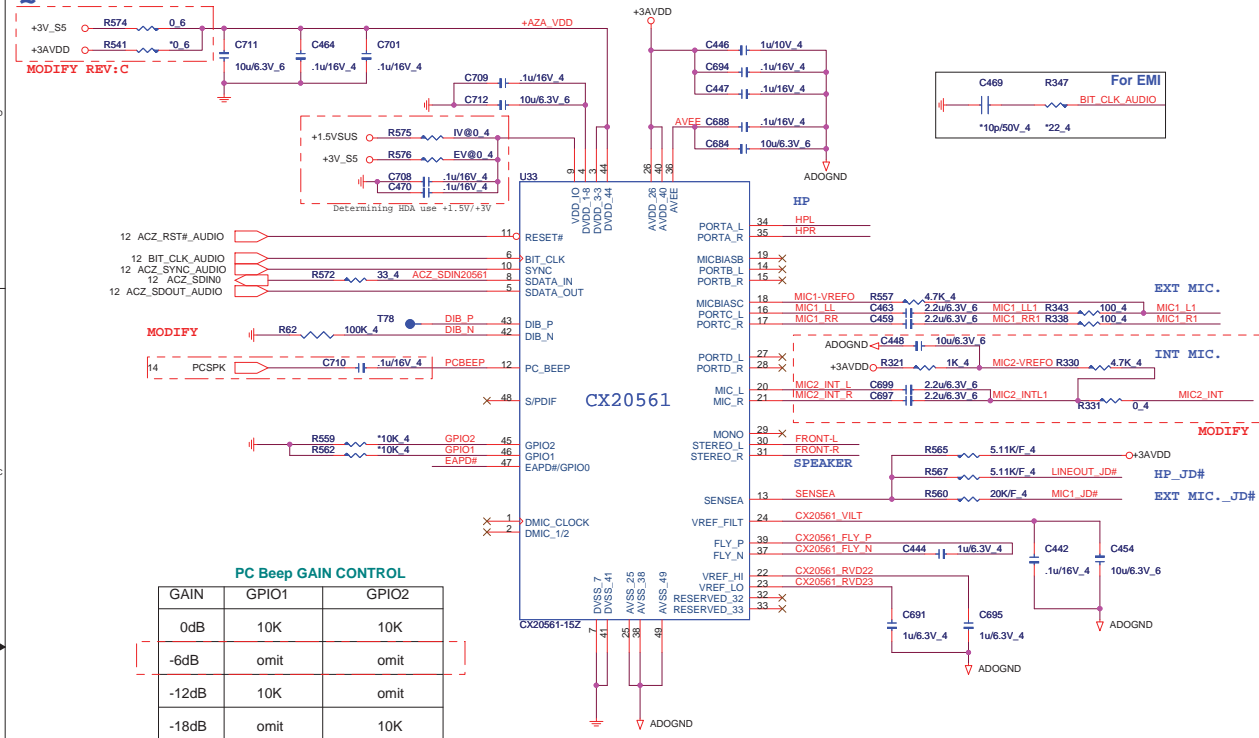


TP CONN

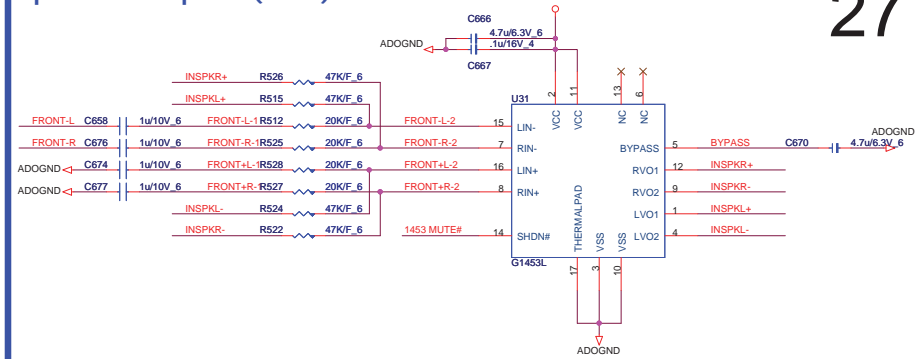


Codec CX20561-15Z (ADO)

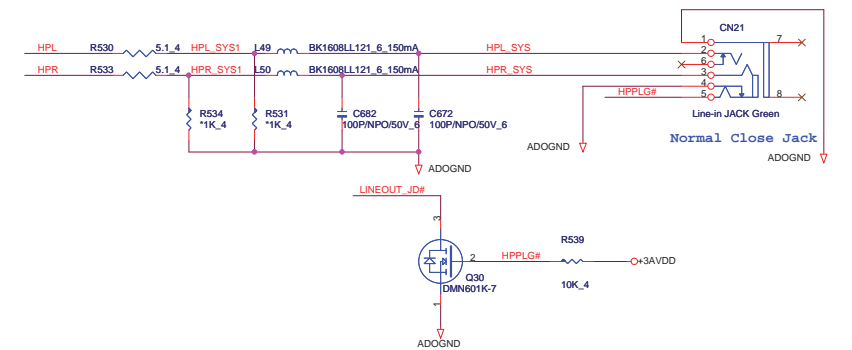
QFN



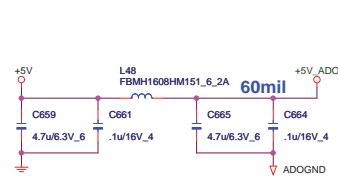
Speaker Amplifier(AMP)



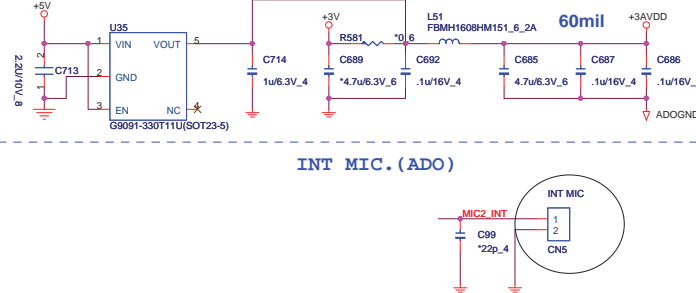
LINE OUT(AMP)



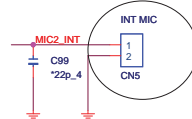
AMP Power(AMP)



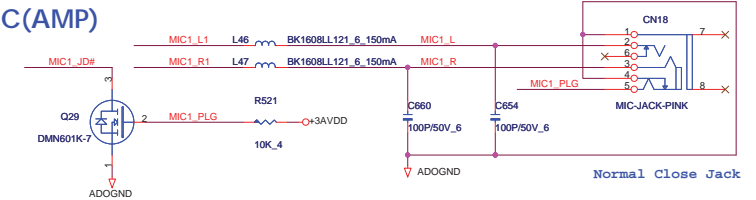
CODER Power(ADO)



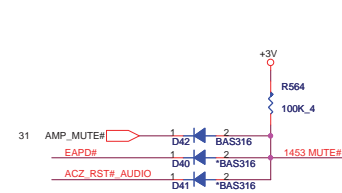
INT MIC. (ADO)



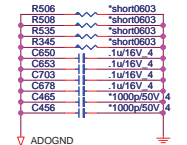
MIC(AMP)



MUTE (AMP)



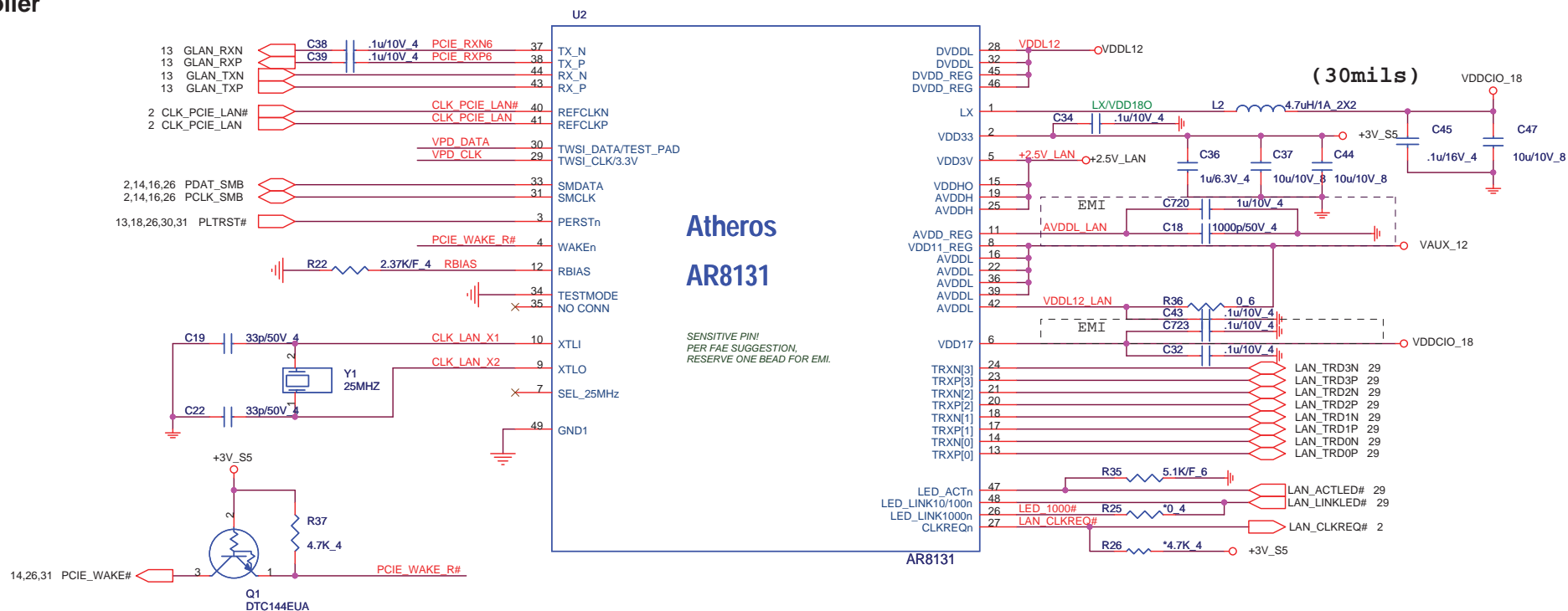
(ADO)



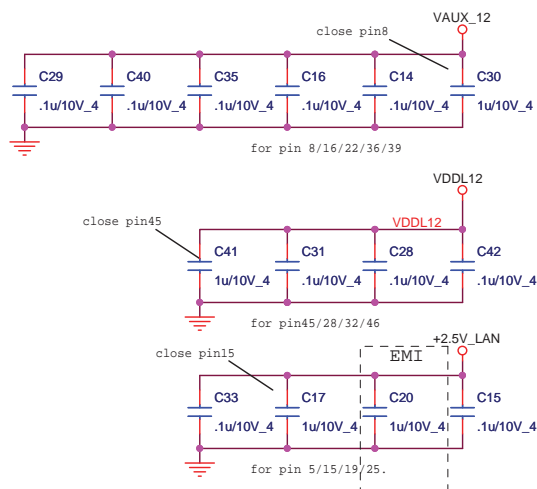
Quanta Computer Inc.

PROJECT : ZR6

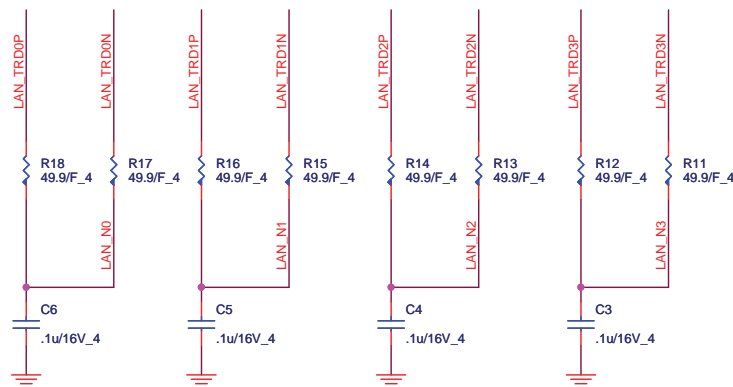
Size Document Number
CODEC/AMP/MDC
 Date: Monday, April 13, 2009 Sheet 27 of 42 Rev 1A



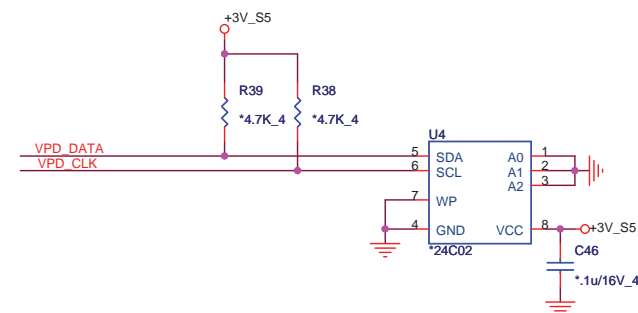
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM

**Quanta Computer Inc.**

PROJECT : ZR6

AR8131 GLAN

Size	Document Number
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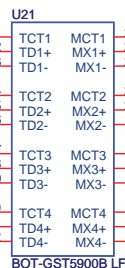
Date: Monday, April 13, 2009

Sheet 28 of 42

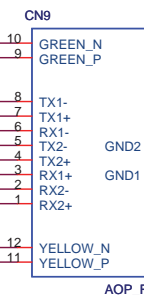
Rev
1A



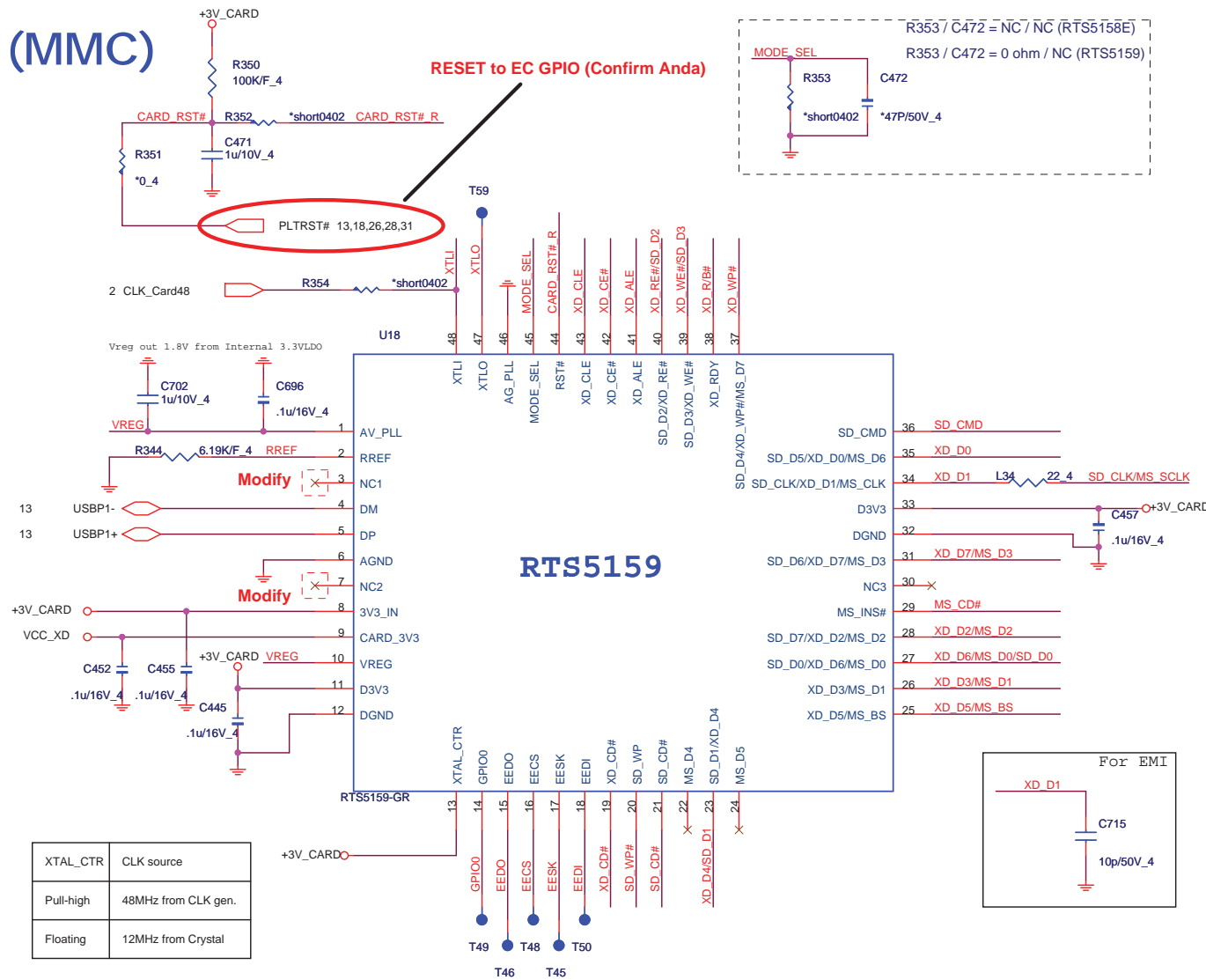
TRANSFORMER



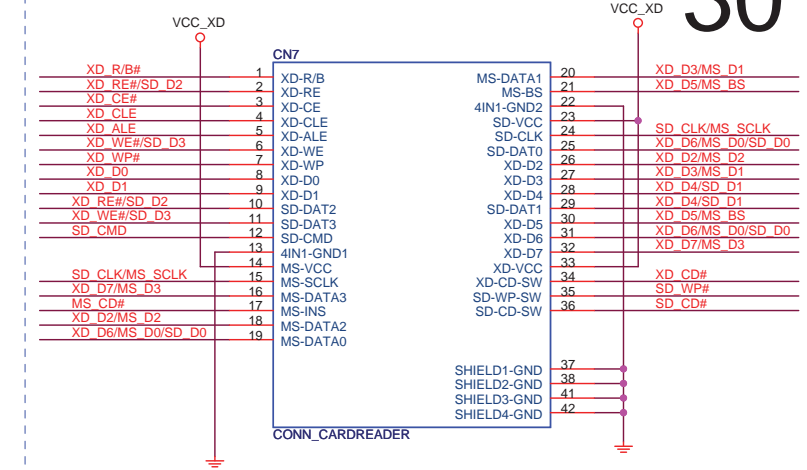
RJ45



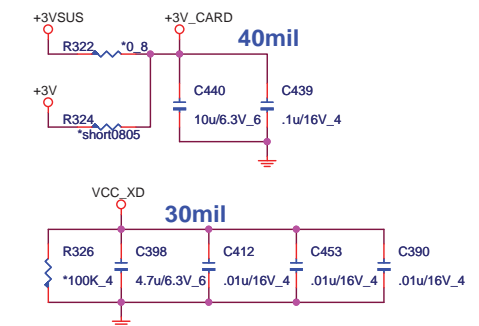
(MMC)



4 IN 1 CARD READER



CARDREADER POWER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal



Quanta Computer Inc.

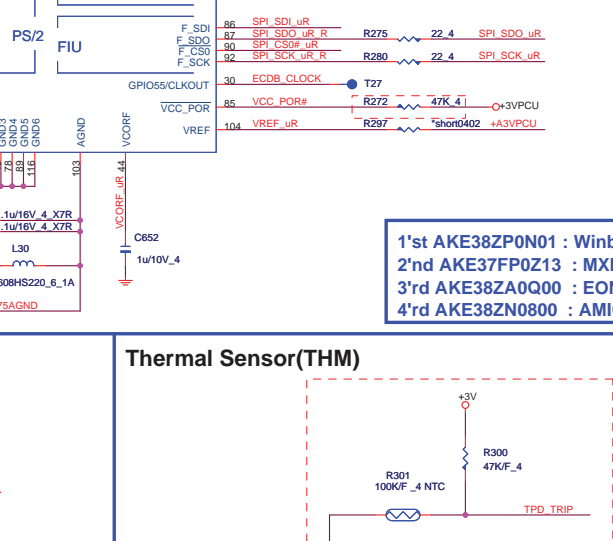
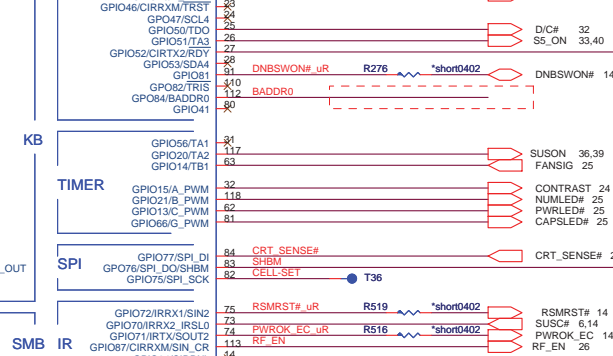
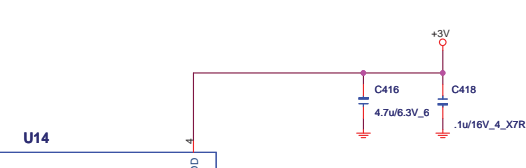
PROJECT : ZR6

Size	Document Number
	CARD READER RTS5159

Rev
1A

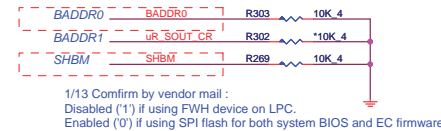
Date: Monday, April 13, 2009

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I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS



MBCLK	R513	4.7K	4
MBDATA	R509	4.7K	4
MXM_SCLK	R304	4.7K	4
MXM_SMDATA	R305	4.7K	4
+3V			
2ND_MBCLK	R259	4.7K	4
2ND_MBDATA	R261	4.7K	4
CRT_SENSE#	R523	4.7K	4

[illegible]

2'nd Source AKE382A0Q00

1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

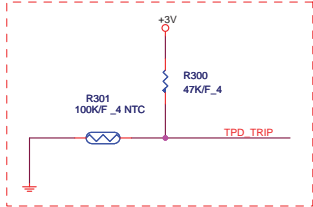
Diagram illustrating the connection between the EV@BAS316 module and the MPWROK 6,14 module. The EV@BAS316 module is connected to the MPWROK 6,14 module via the following pins and components:

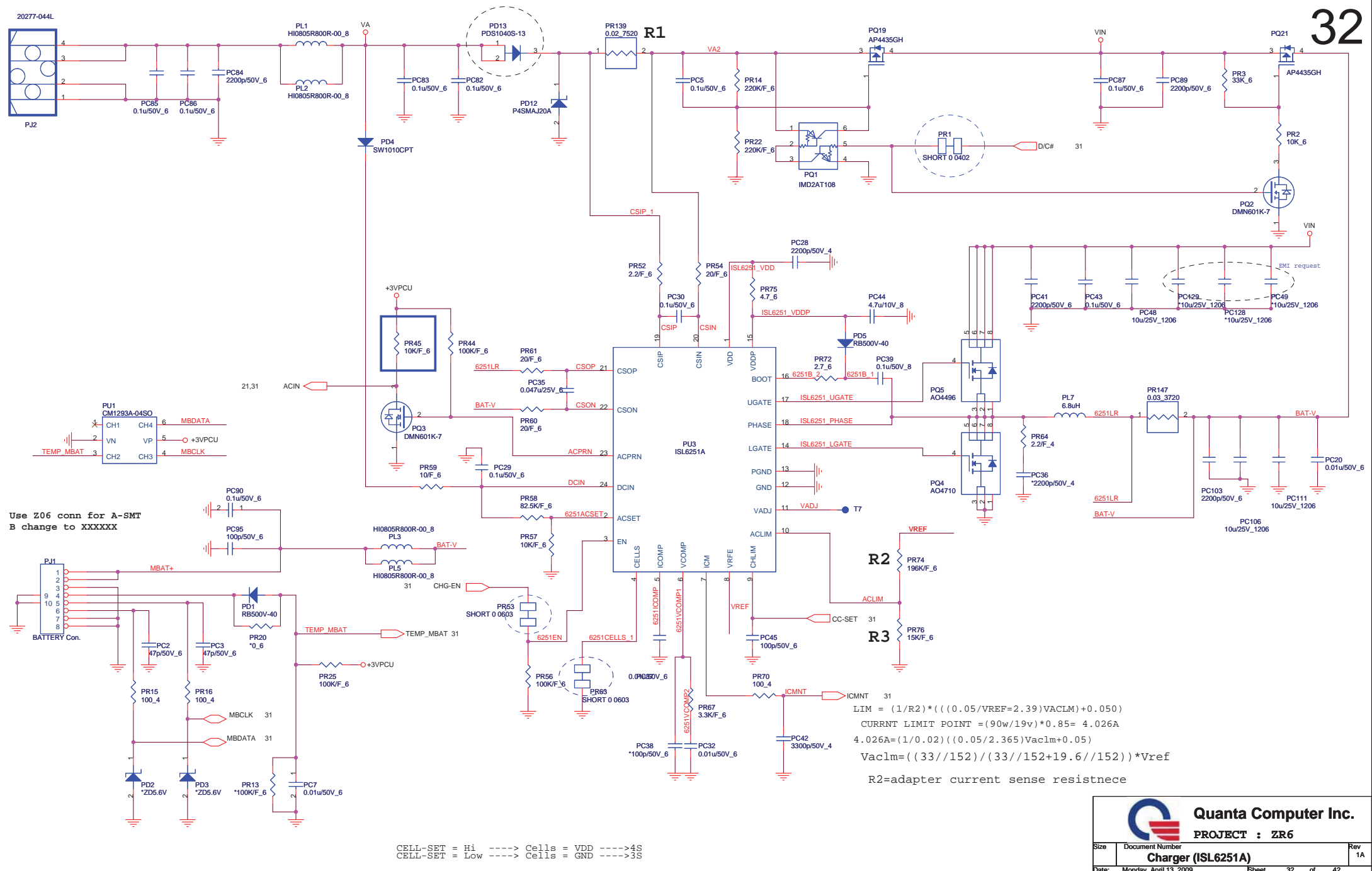
- EV@BAS316 Pin D19** is connected to **MPWROK 6,14 Pin 37 (1V8_ON)**.
- EV@BAS316 Pin D24** is connected to **MPWROK 6,14 Pin 6,36 (HWPG_1.5V)**.
- EV@BAS316 Pin D20** is connected to **MPWROK 6,14 Pin 34 (HWPG_1.05V)**.
- EV@BAS316 Pin D25** is connected to **MPWROK 6,14 Pin 38,39 (HWPG_1.8V)**.
- EV@BAS316 Pin D21** is connected to **MPWROK 6,14 Pin 33 (SYS_HWPG)**.
- EV@BAS316 Pin D22** is connected to **MPWROK 6,14 Pin 3,6,14,35 (DELAY_VR_PWPGOOD)**.
- EV@BAS316 Pin D23** is connected to **MPWROK 6,14 Pin 37 (HWPG_1.1V)**.

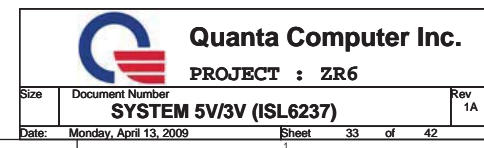
Additional components shown in the diagram include:

- R273** (10K_4) connected to the EV@BAS316 module.
- R263** (short0402) connected to the MPWROK 6,14 module.

INTERNAL KEYBOARD STRIP SET



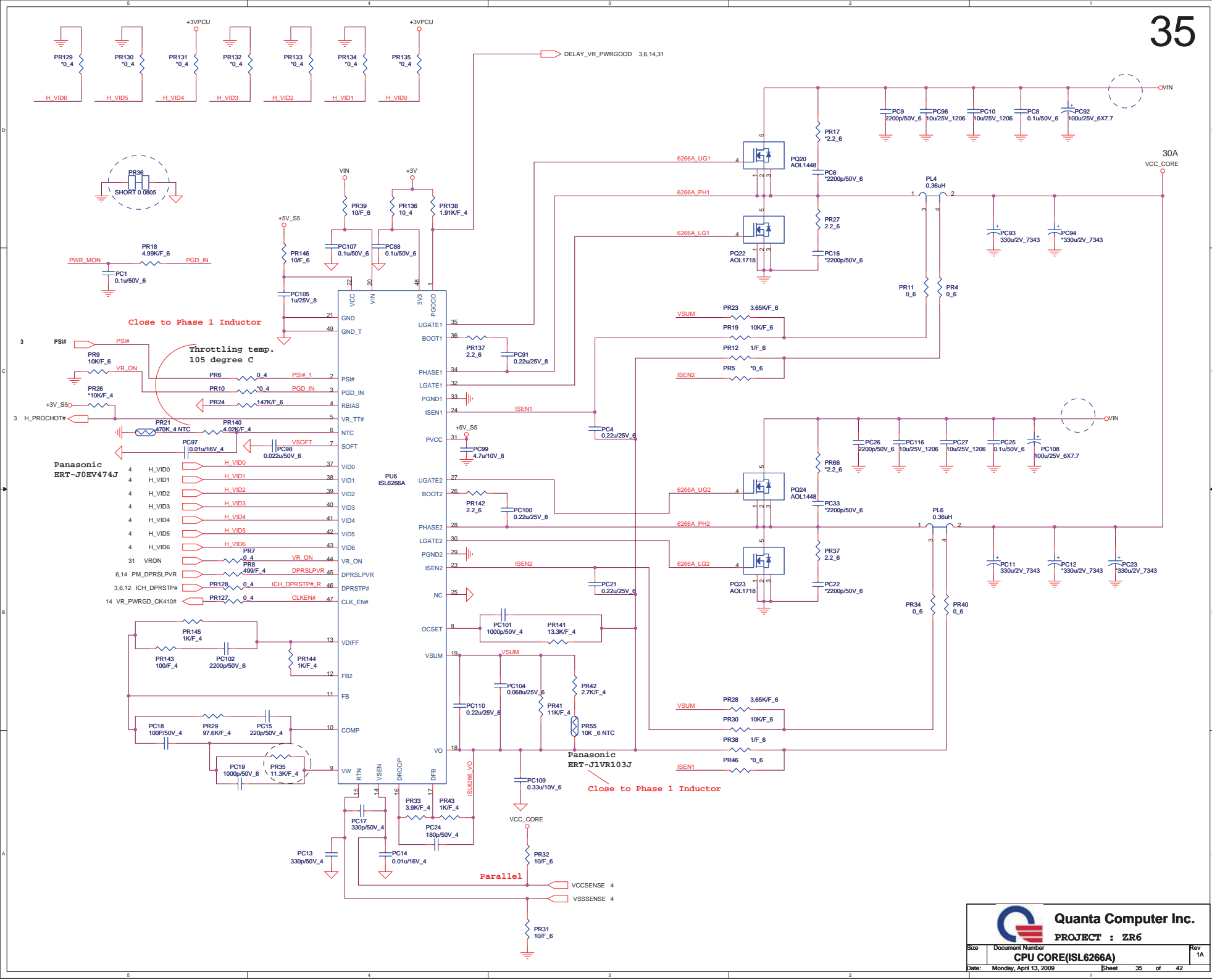


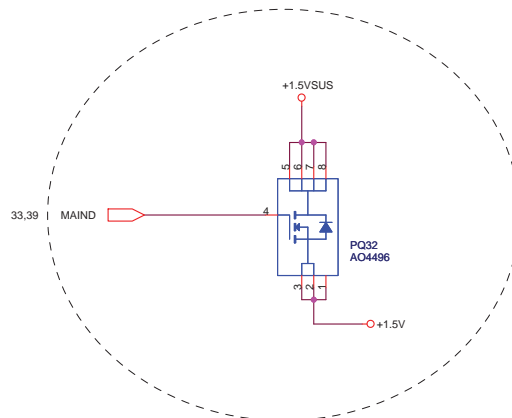




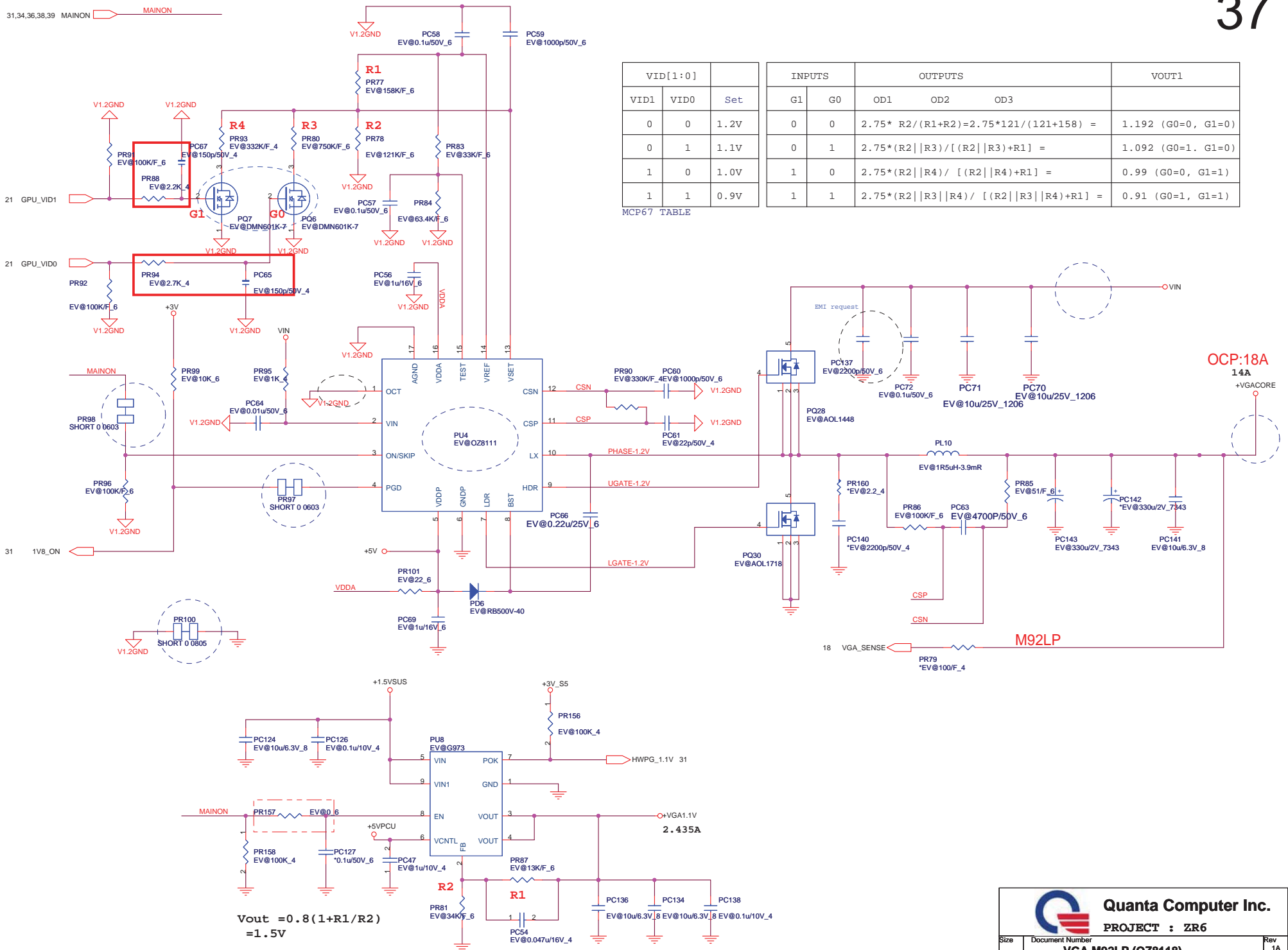
A circuit diagram showing a voltage source labeled **+1.05V** connected to a capacitor labeled **PC125 0.1u/50V_6**. The capacitor is connected to ground, represented by a red ground symbol at the bottom.



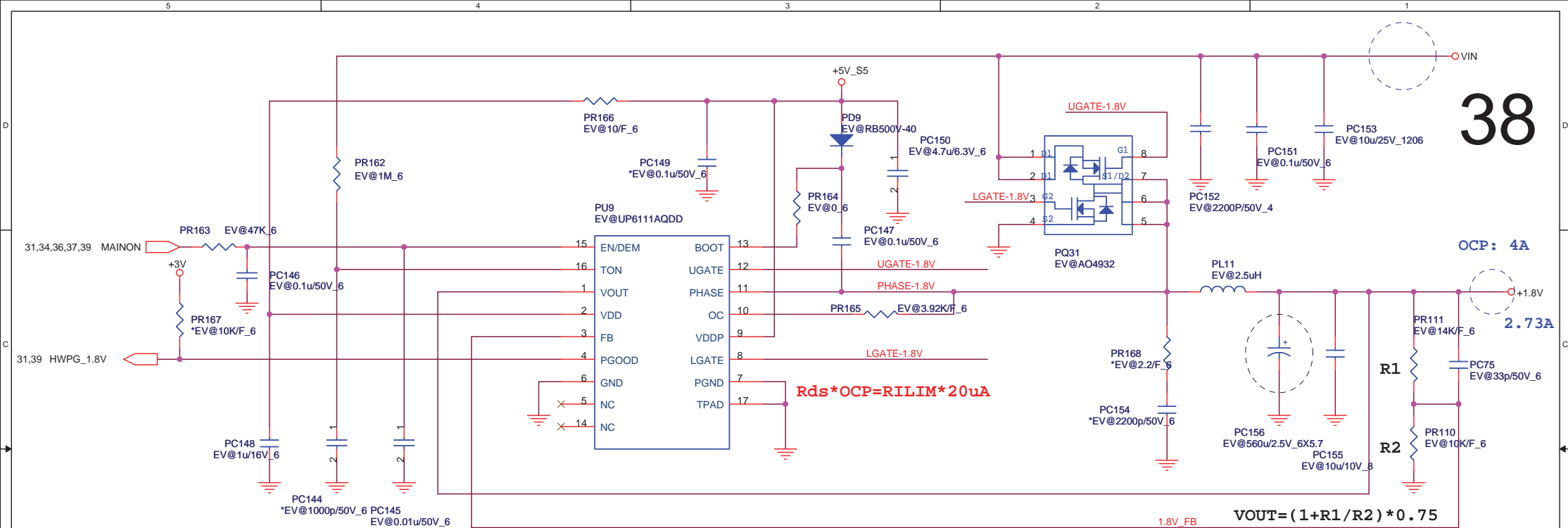




31,34,36,38,39 MAINON



38



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

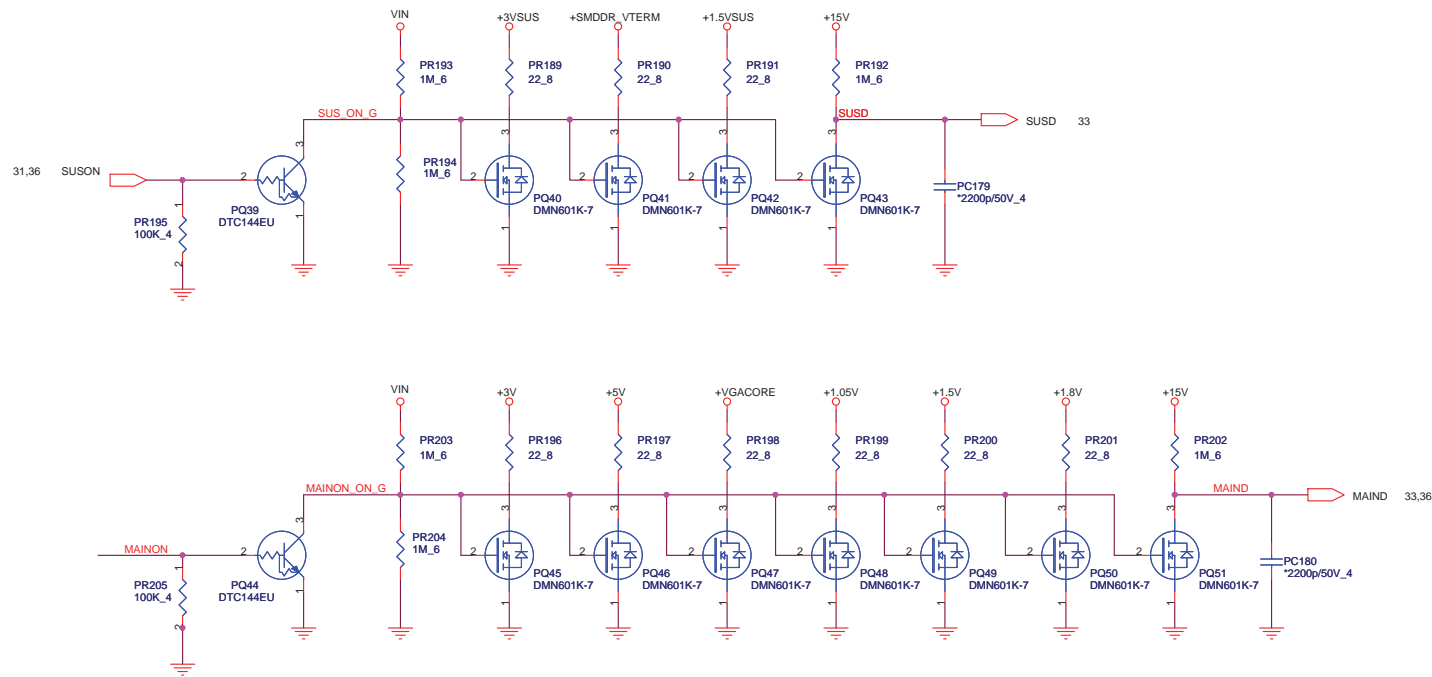
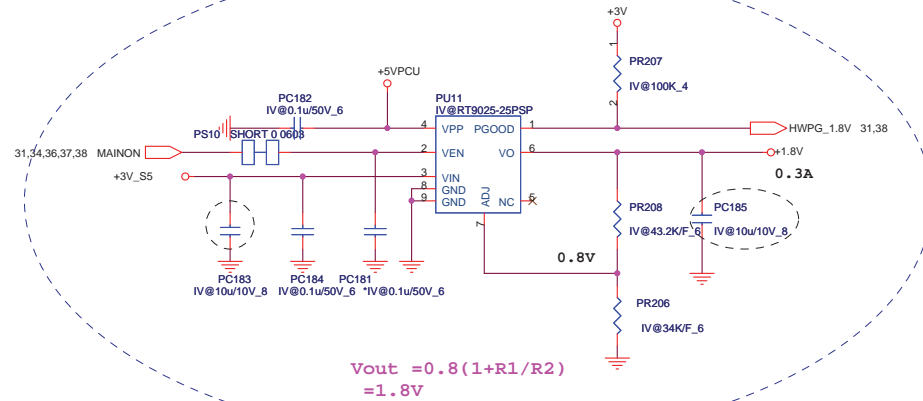
AO4932 Rds=15.6~19.6mOhm

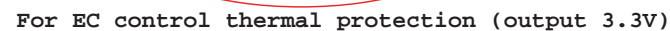
OCP=16-0.8A

$$L(ripple\ current) = (19 - 1.8) * 1.8 / (2.5u * 272k * 19) \\ \sim 2.14A$$

$$19.6m * 4 = RILIM * 20uA$$


$$RILIM = 3.92K$$





[illegible]

MODEL: REV		CHANGE LIST	MODEL		
			ZR6 MB		
PAGE			FROM	TO	
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request	1	1A	
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS	2	1A	
		Page3:Del Q5,Q6,R62,R63	3	1A	
		Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH	4	1A	
		Page21:Del Q10,Q9,R96,R86	5	2A	
		Page27:R574 stuff and R541 no stuff	6	1A	
		Page31:R300,R301 stuff thermal sensor	7	1A	
		Page37:change PC65,PC67 to 150pF	8	1A	
		Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip)	9	3A	
		Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone	10	3A	
		Page27:change CN8 (usb) 12 pin board to board	11	1A	
		Page26:Change CN5 footprint to cwy027-b0glz-2p-1,CN16(USB)footprint change to usb-c107h6-10405-1-4p-r-v-nb4	12	1A	
		Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4	13	1A	
		Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4	14	3A	
		Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2	15	2A	
		Page04:change C493 to no stuff	16	1A	
		Page27:Del T77 and Add R62	17	3A	
		Page26:change Hole21 footprint to h-c236d142pt-8	18	2A	
		Page24:Change D1 `D2 `D3 footprint to led-ht-110nb5-3p	19	3A	
		Page24:Change R218,R234 to shortpad	20	1A	
		Page26:Change R310 to shortpad	21	3A	
		Page10:Change R91,R307,R418,R466,R469 to shortpad	22	1A	
		Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND	23	3A	
		Page26:Add C716 for EMI	24	3A	
		Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1%	25	2A	
		Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number	26	3A	
		Page14:Change R282 to no stuff	27	2A	
		Page28:Change R26 to no stuff	28	3A	
		Page26:Change Hole29 part number to MBZR6005010	29	3A	
		Page29:Del net name LAN_LNK_LED_FWR	30	1A	
		D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff	31	3A
			Page24:change HDMI item to no stuff(remove this function)	32	2A
			Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio	33	2A
			Page26:Change Hole 16 footprint as hole1	34	2A
				35	2A
				36	2A
				37	2A
		E	Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62	38	2A
			Page27:C670 change value from 1U to 4.7U (CH5471M9907)	39	3A
			Page29:change c478 from 1000p to 220p.(CH122GKI10)	40	3B
			Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93) ,ADD C720 1u (CH5102K9B06)		
	Page25:change DHP00DA1G03->DHPTME53201				
	Page24:add C722 (CH6101M9905) to solve ISN issue				
	Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM.				
	Page34:change PC133 from CC7560JNZ15 to CC7560JNZ02 for cost down				
	Page36:change PC139 from CC7560JNZ15 to CC7560JNZ02 for cost down				
	Page38:change PC156 from CC7560JNZ15 to CC7560JNZ02 for cost down				
	Page33:change PC158,PC162 from CC73301MVB2 to CC73301MZ04 for cost down				
	Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down				
	MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70		Project :ZR6 MB	Document No.:	
Approved by : Johnny_O		Drawing by :Andy Chen	DATE: 2009/03/04		



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Thermal Protection

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